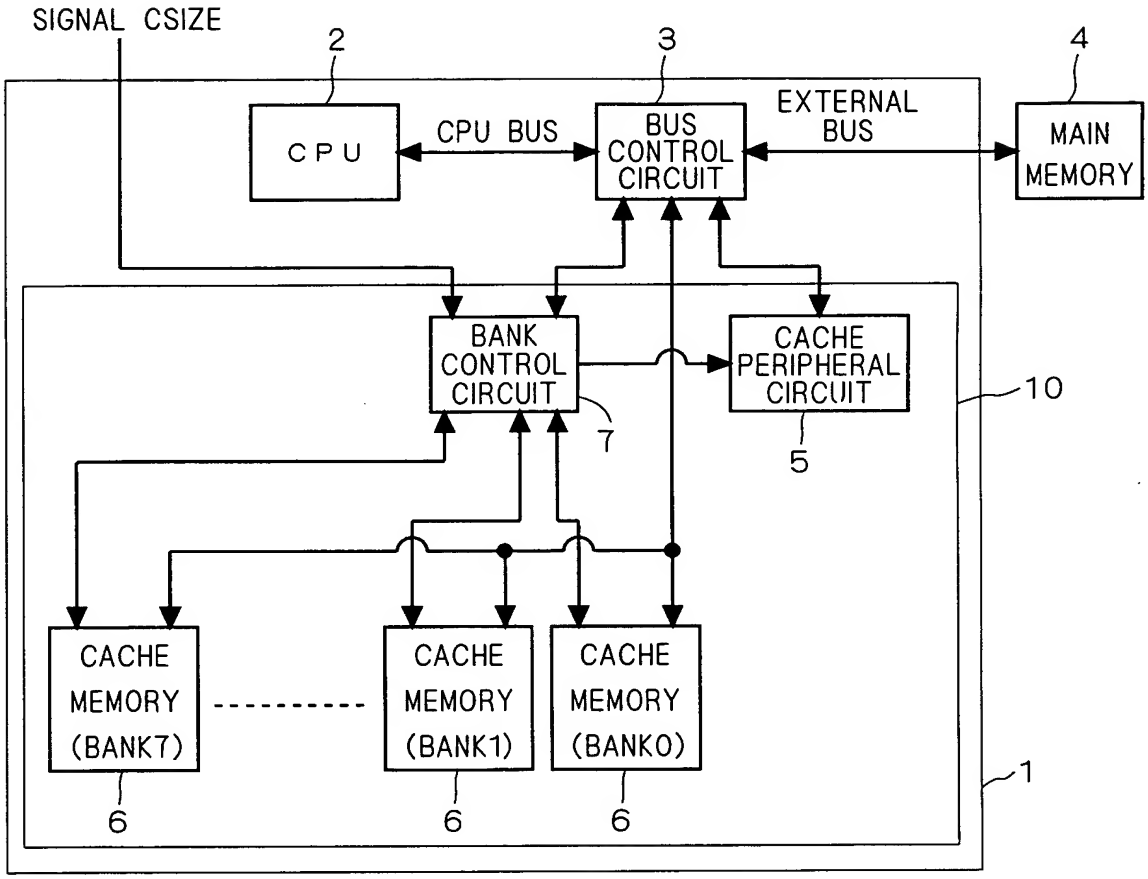
FIG. 1


SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANK7)
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK0)
6
6
6
1

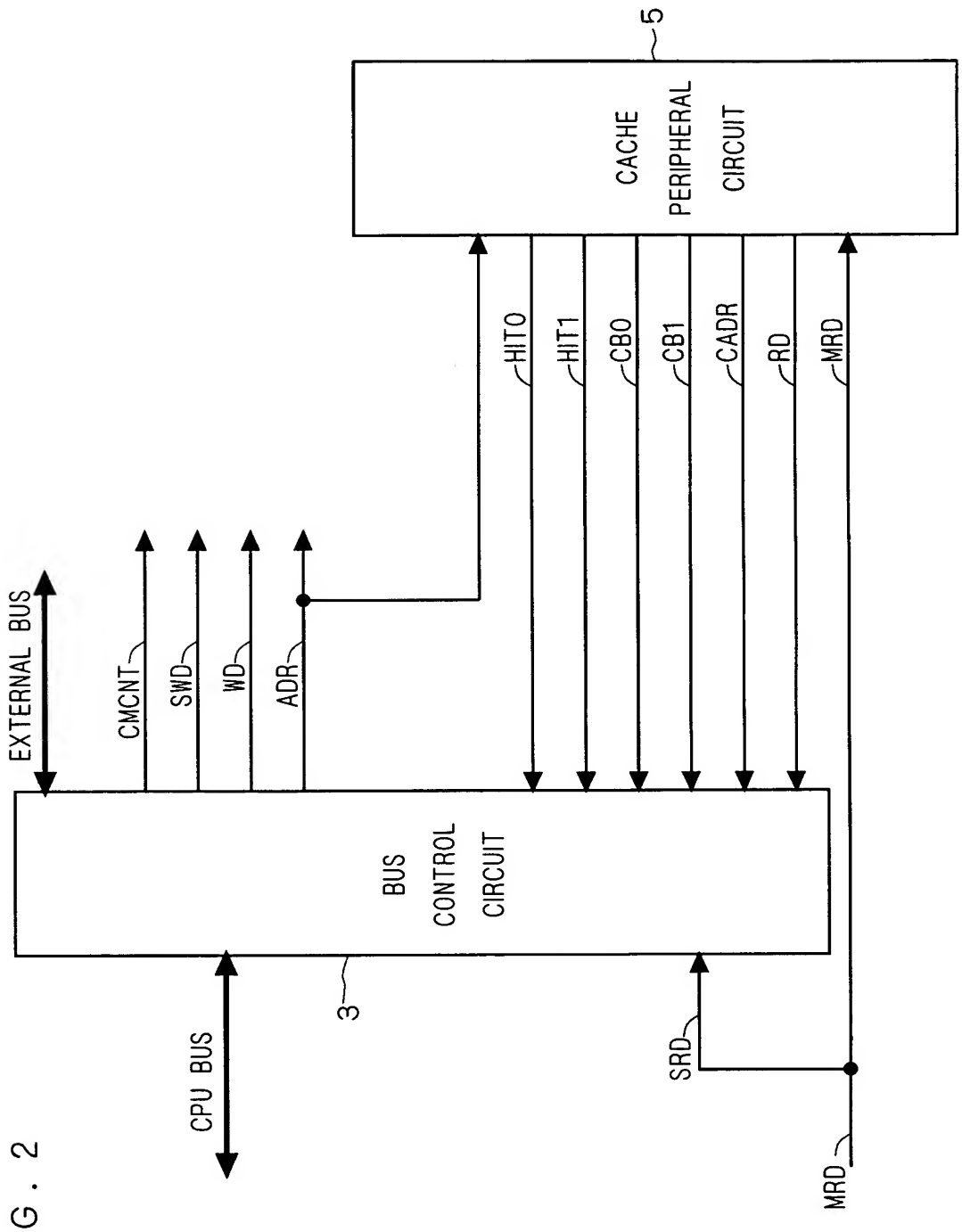

5
CACHE PERIPHERAL CIRCUIT
HIT0
HIT1
CB0
CB1
CADR
RD
MRD
EXTERNAL BUS
CMCNT
SWD
WD
ADR
BUS CONTROL CIRCUIT
3
CPU BUS
SRD
MRD

FIG. 2

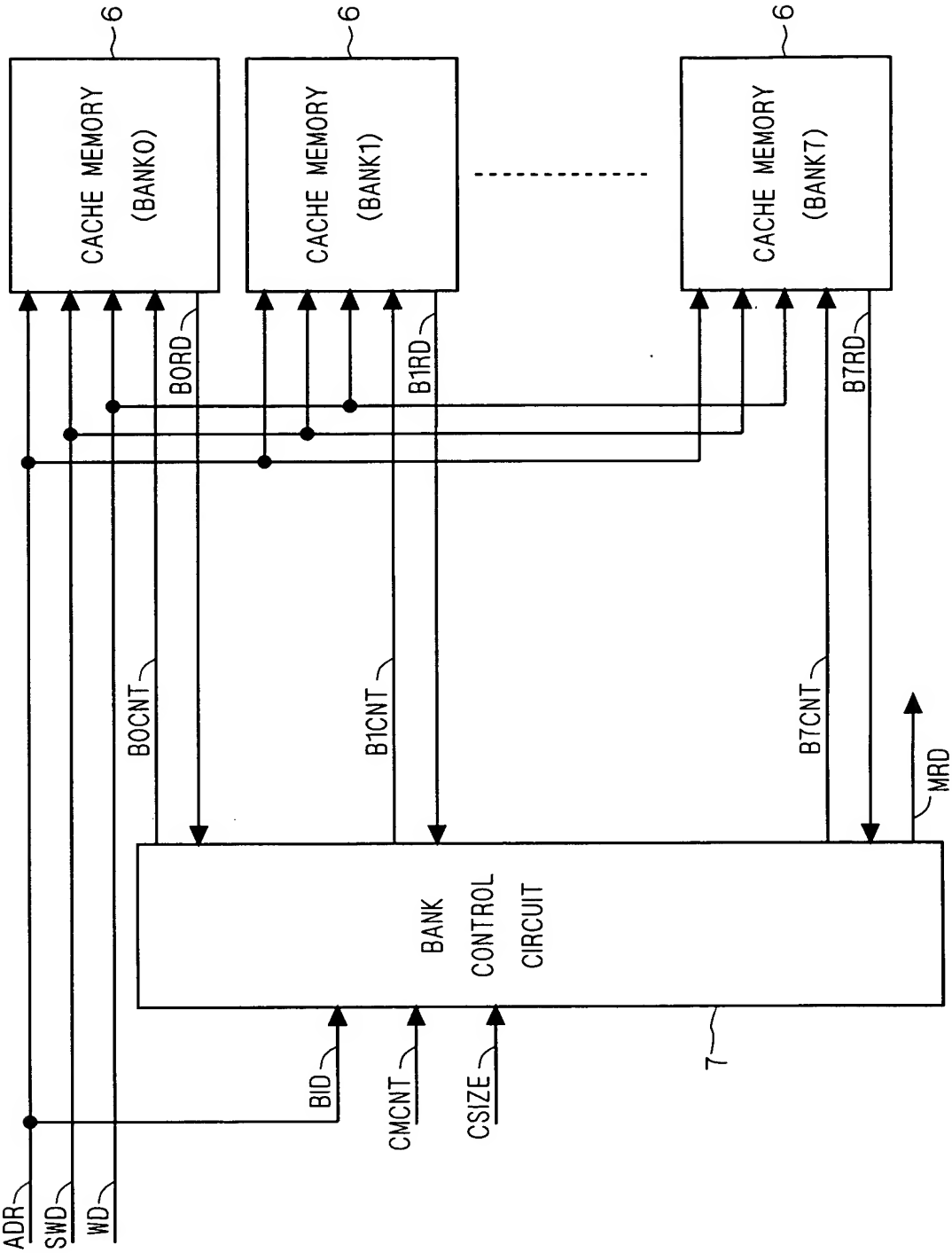

6
6
6
CACHE MEMORY (BANK0)
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK7)
B0RD
B1RD
B7RD
B0CNT
B1CNT
B7CNT
MRD
BANK CONTROL CIRCUIT
7
BID
CMCNT
CSIZE
ADR
SWD
WD

FIG. 3

FIG. 4

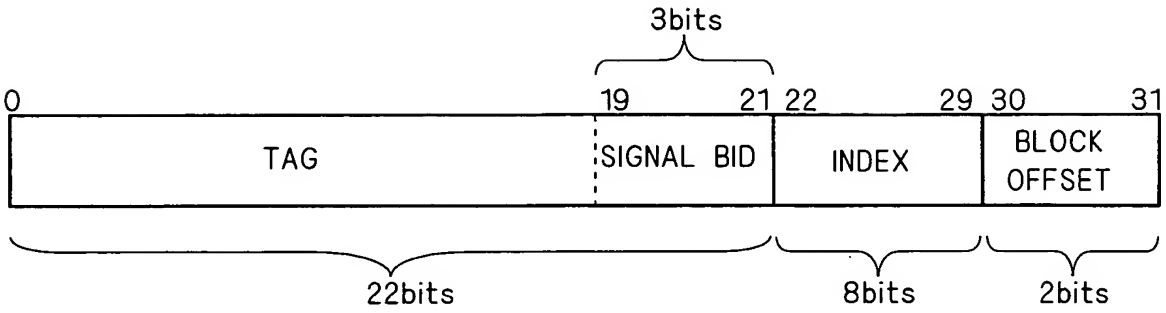

3bits
0
19
21
22
29
30
31
TAG
SIGNAL BID
INDEX
BLOCK OFFSET
22bits
8bits
2bits

FIG. 5

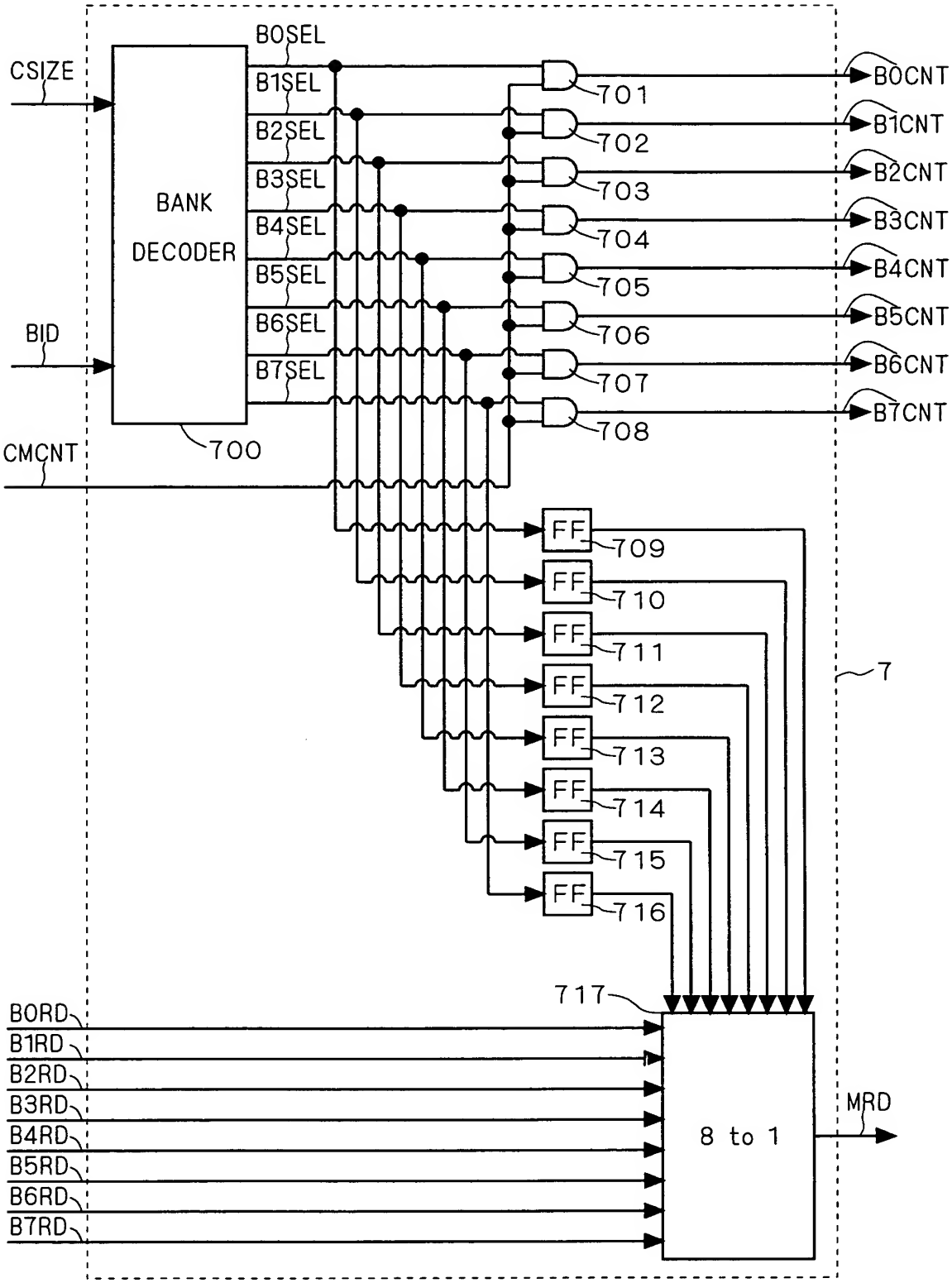

CSIZE
BID
CMCNT
BANK
DECODER
700
B0SEL
B1SEL
B2SEL
B3SEL
B4SEL
B5SEL
B6SEL
B7SEL
701
702
703
704
705
706
707
708
B0CNT
B1CNT
B2CNT
B3CNT
B4CNT
B5CNT
B6CNT
B7CNT
FF
709
710
711
712
713
714
715
716
7
717
B0RD
B1RD
B2RD
B3RD
B4RD
B5RD
B6RD
B7RD
8 to 1
MRD

FIG. 6

CSIZE	BID	BANK0 SELECTION SIGNAL	BANK1 SELECTION SIGNAL	BANK2 SELECTION SIGNAL	BANK3 SELECTION SIGNAL	BANK4 SELECTION SIGNAL	BANK5 SELECTION SIGNAL	BANK6 SELECTION SIGNAL	BANK7 SELECTION SIGNAL
00	000	1	0	0	0	0	0	0	0
	001	1	0	0	0	0	0	0	0
	010	1	0	0	0	0	0	0	0
	011	1	0	0	0	0	0	0	0
	100	1	0	0	0	0	0	0	0
	101	1	0	0	0	0	0	0	0
	110	1	0	0	0	0	0	0	0
	111	1	0	0	0	0	0	0	0
01	000	1	0	0	0	0	0	0	0
	001	0	1	0	0	0	0	0	0
	010	1	0	0	0	0	0	0	0
	011	0	1	0	0	0	0	0	0
	100	1	0	0	0	0	0	0	0
	101	0	1	0	0	0	0	0	0
	110	1	0	0	0	0	0	0	0
	111	0	1	0	0	0	0	0	0
10	000	1	0	0	0	0	0	0	0
	001	0	1	0	0	0	0	0	0
	010	0	0	1	0	0	0	0	0
	011	0	0	0	1	0	0	0	0
	100	1	0	0	0	0	0	0	0
	101	0	1	0	0	0	0	0	0
	110	0	0	1	0	0	0	0	0
	111	0	0	0	1	0	0	0	0
11	000	1	0	0	0	0	0	0	0
	001	0	1	0	0	0	0	0	0
	010	0	0	1	0	0	0	0	0
	011	0	0	0	1	0	0	0	0
	100	0	0	0	0	1	0	0	0
	101	0	0	0	0	0	1	0	0
	110	0	0	0	0	0	0	1	0
	111	0	0	0	0	0	0	0	1

OBLON, SPIVAK, ET AL
DOCKET # 243970US2
INV: Takashi KURAFUJI
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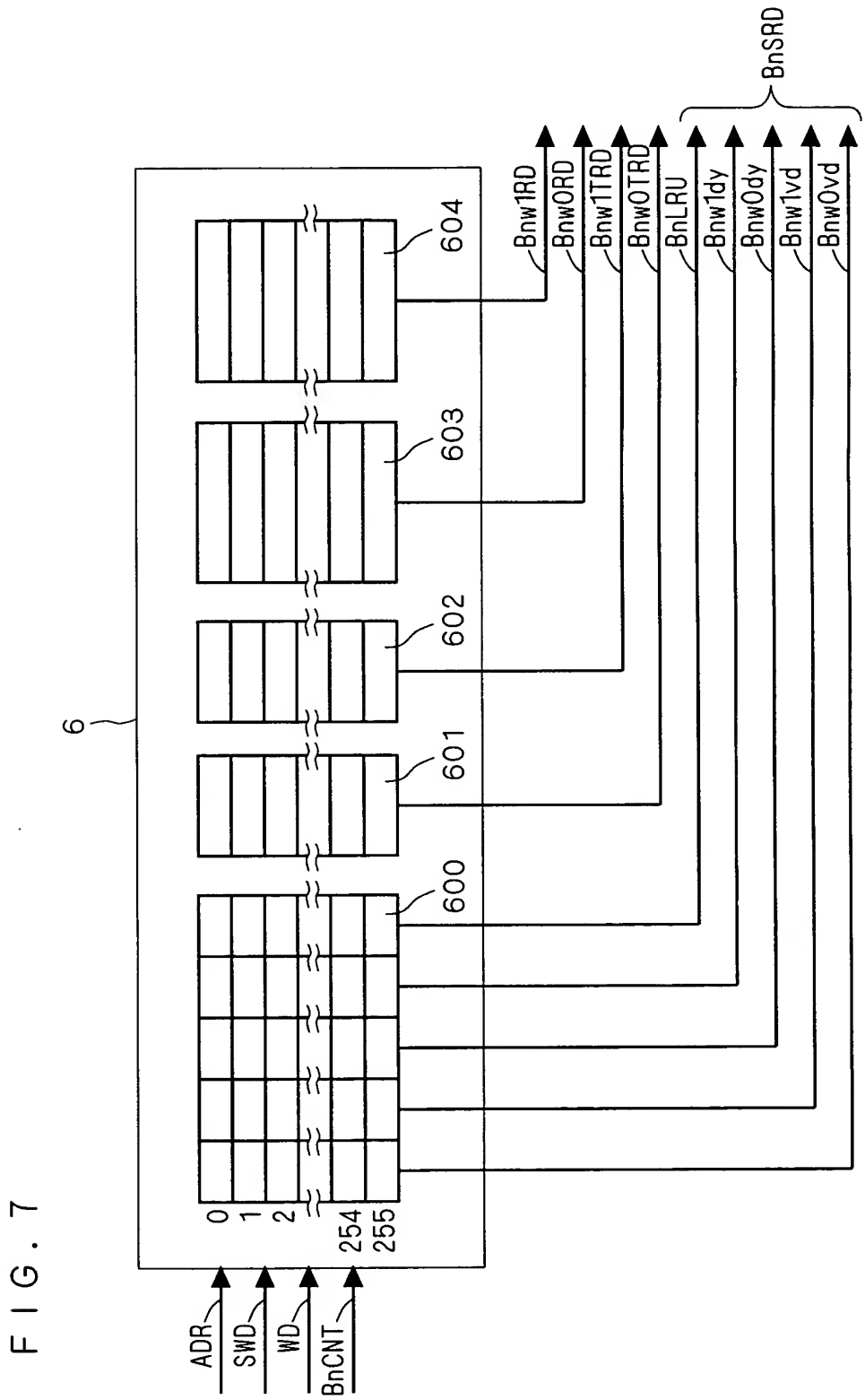

BnSRD
BnwIRD
BnwORD
BnwITRD
BnwOTRD
BnLRU
Bnw1dy
BnwOdy
Bnw1vd
BnwOvd
604
603
602
601
600
6
0
1
2
254
255
ADR
SWD
WD
BnCNT

FIG. 7

FIG. 8

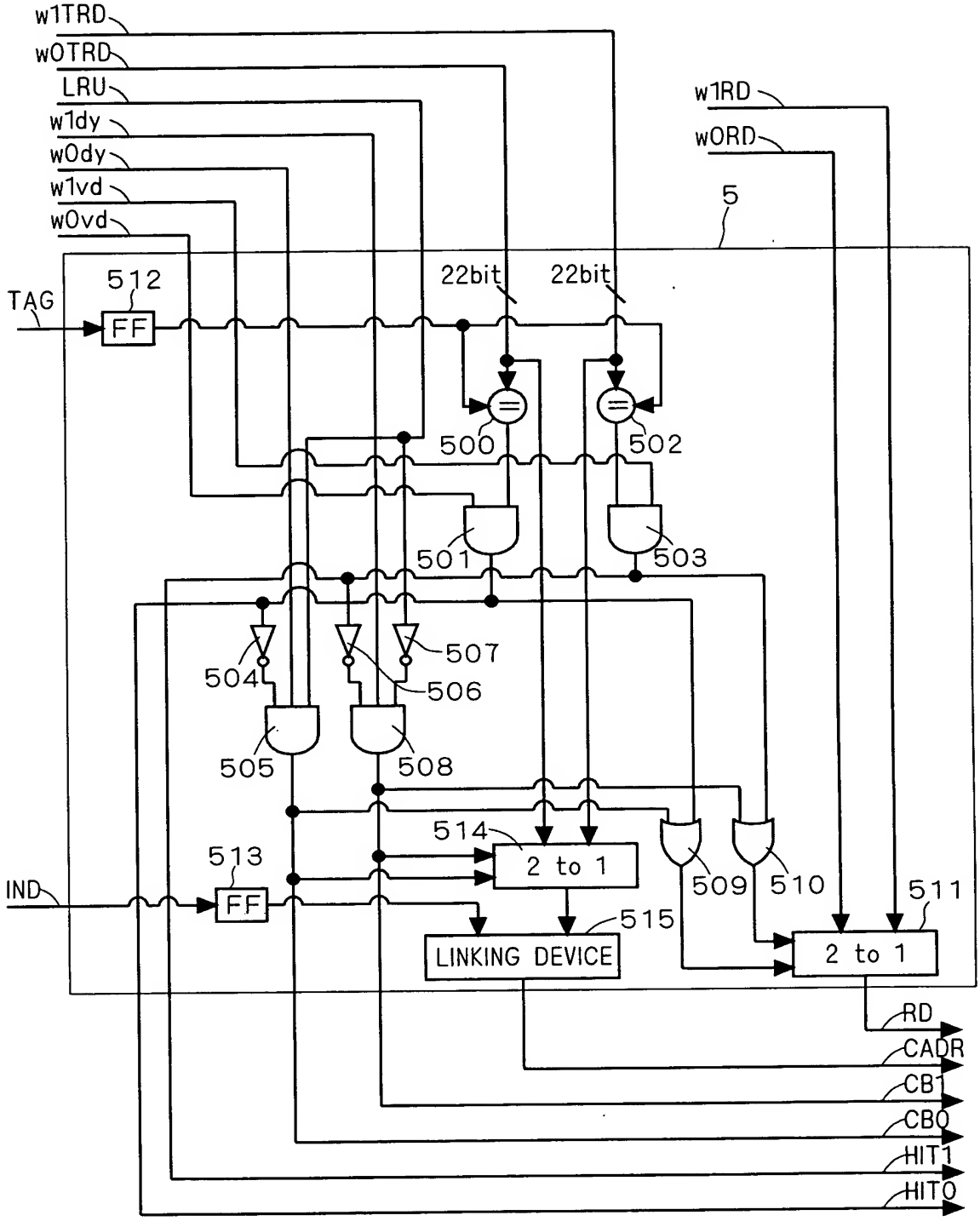

w1TRD
w0TRD
LRU
w1dy
w0dy
w1vd
w0vd
w1RD
w0RD
5
TAG
512
FF
22bit
22bit
500
502
501
503
504
507
506
505
508
514
2 to 1
513
IND
FF
509
510
511
515
LINKING DEVICE
2 to 1
RD
CADR
CB1
CB0
HIT1
HIT0

FIG. 9

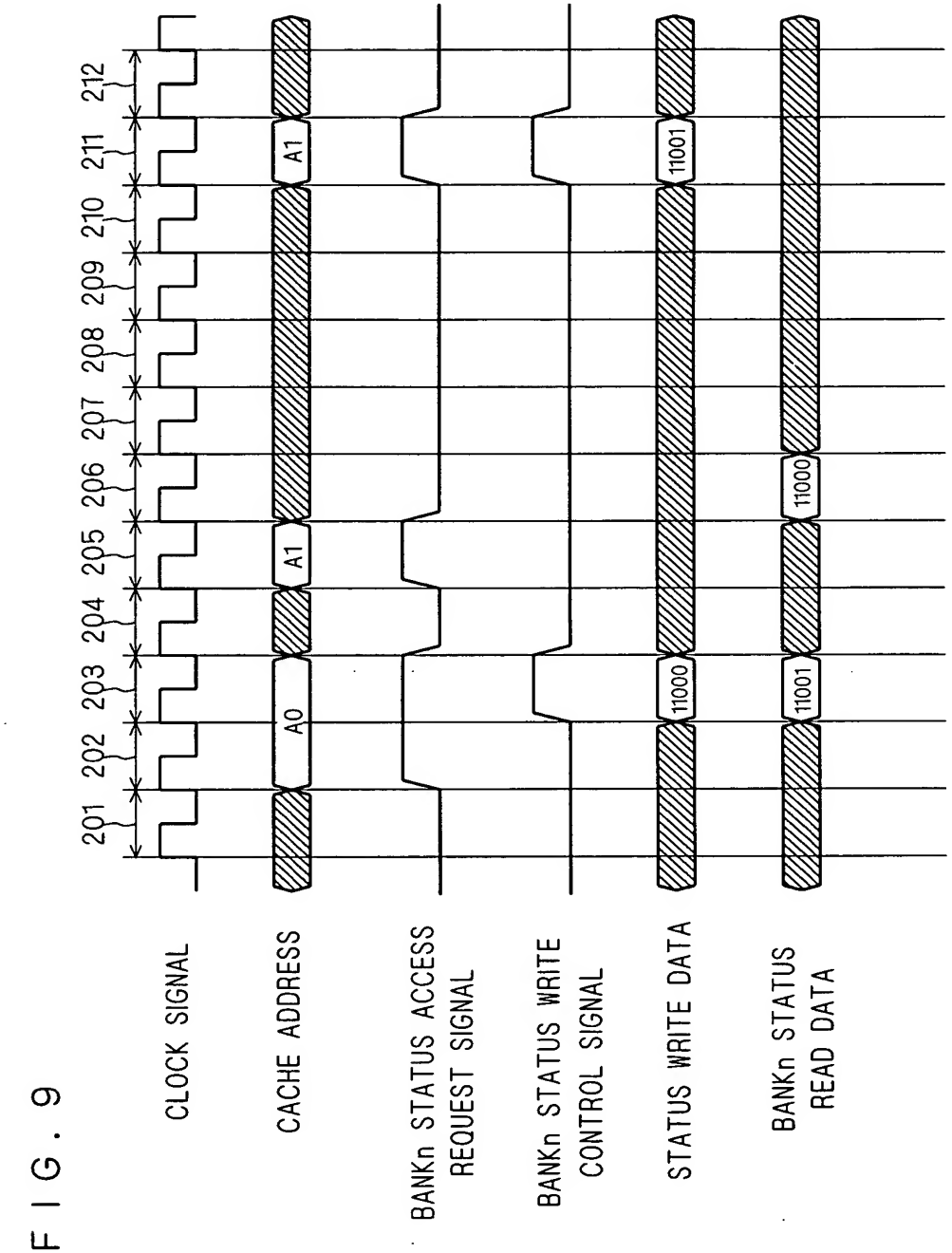

201
202
203
204
205
206
207
208
209
210
211
212
CLOCK SIGNAL
CACHE ADDRESS
A0
A1
A1
BANKn STATUS ACCESS REQUEST SIGNAL
BANKn STATUS WRITE CONTROL SIGNAL
STATUS WRITE DATA
11000
11001
BANKn STATUS READ DATA
11001
11000

FIG. 10

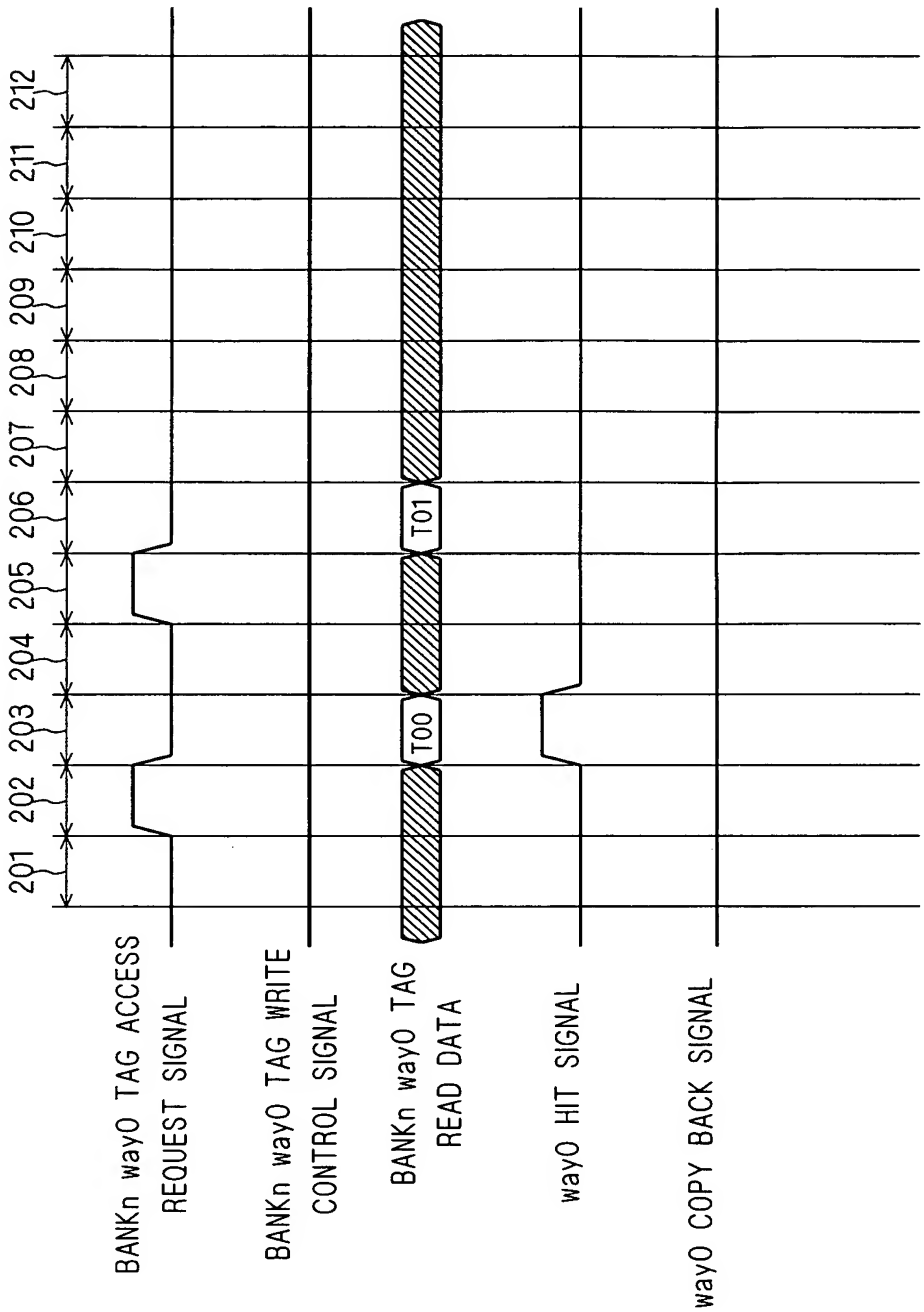

201
202
203
204
205
206
207
208
209
210
211
212
T00
T01
BANKn way0 TAG ACCESS REQUEST SIGNAL
BANKn way0 TAG WRITE CONTROL SIGNAL
BANKn way0 TAG READ DATA
way0 HIT SIGNAL
way0 COPY BACK SIGNAL

FIG. 11

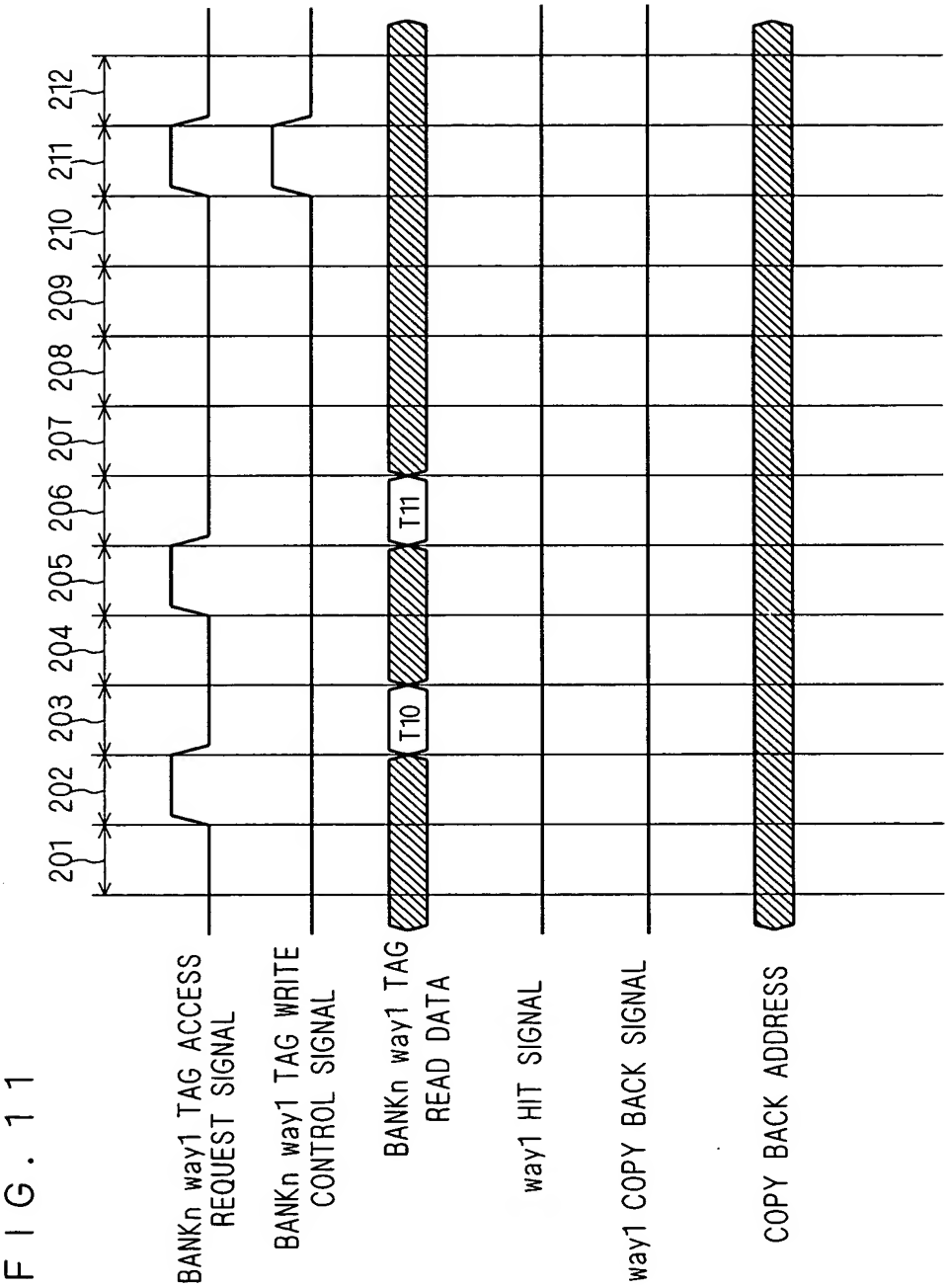

201
202
203
204
205
206
207
208
209
210
211
212
BANKn way1 TAG ACCESS REQUEST SIGNAL
BANKn way1 TAG WRITE CONTROL SIGNAL
BANKn way1 TAG READ DATA
T10
T11
way1 HIT SIGNAL
way1 COPY BACK SIGNAL
COPY BACK ADDRESS

FIG. 12

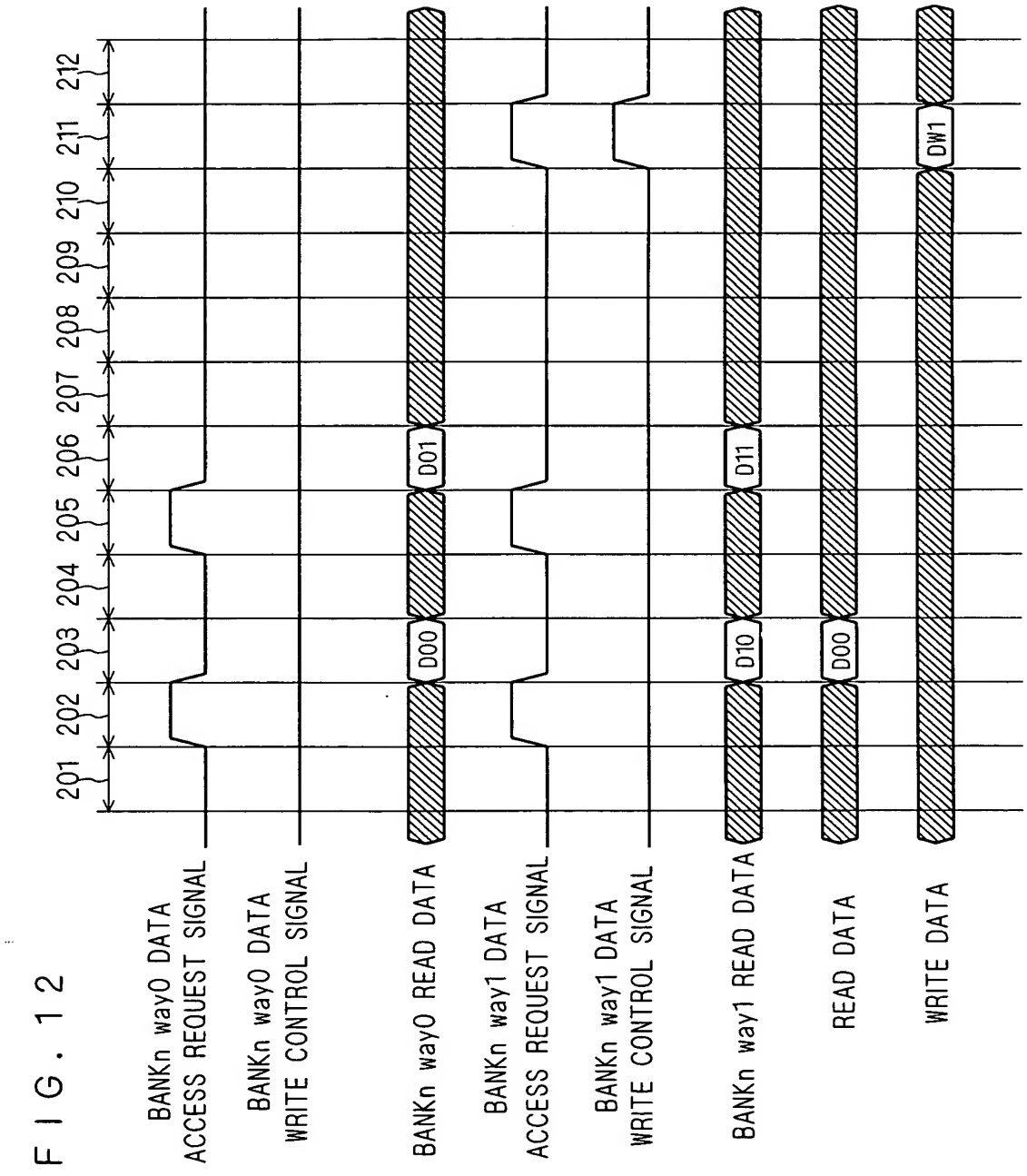

201
202
203
204
205
206
207
208
209
210
211
212
BANKn way0 DATA ACCESS REQUEST SIGNAL
BANKn way0 DATA WRITE CONTROL SIGNAL
BANKn way0 READ DATA
BANKn way1 DATA ACCESS REQUEST SIGNAL
BANKn way1 DATA WRITE CONTROL SIGNAL
BANKn way1 READ DATA
READ DATA
WRITE DATA
D00
D01
D10
D11
D00
DW1

FIG. 13

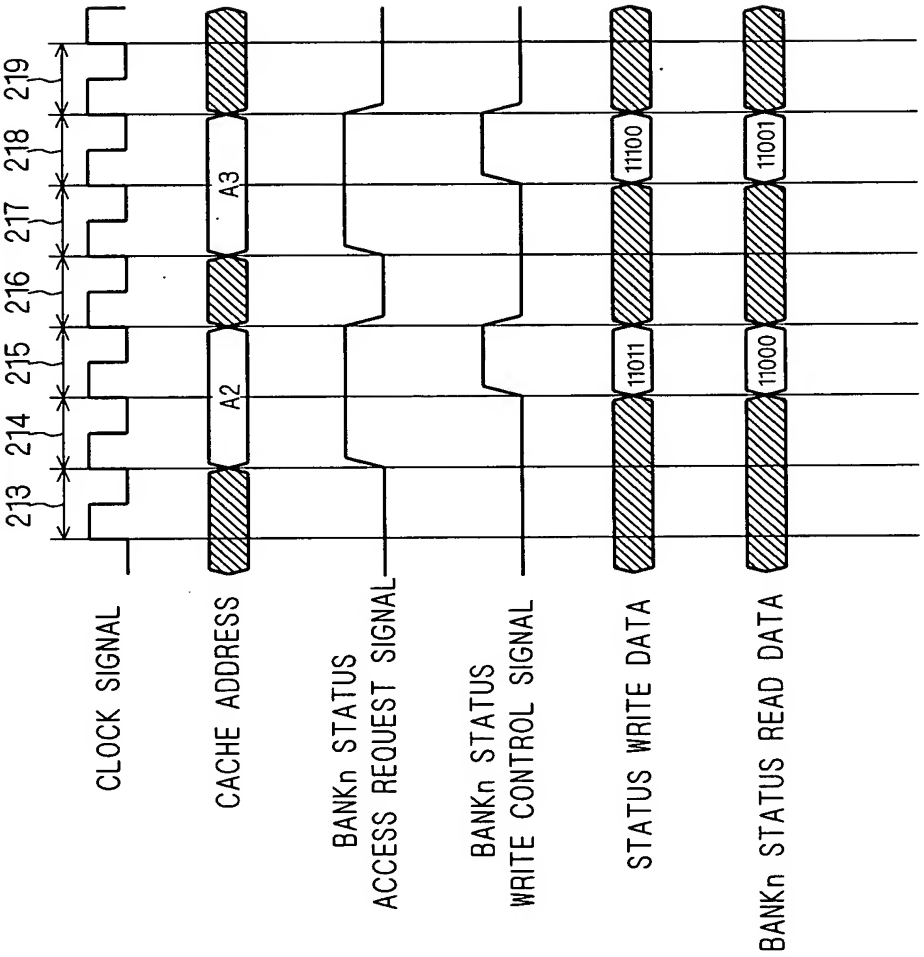
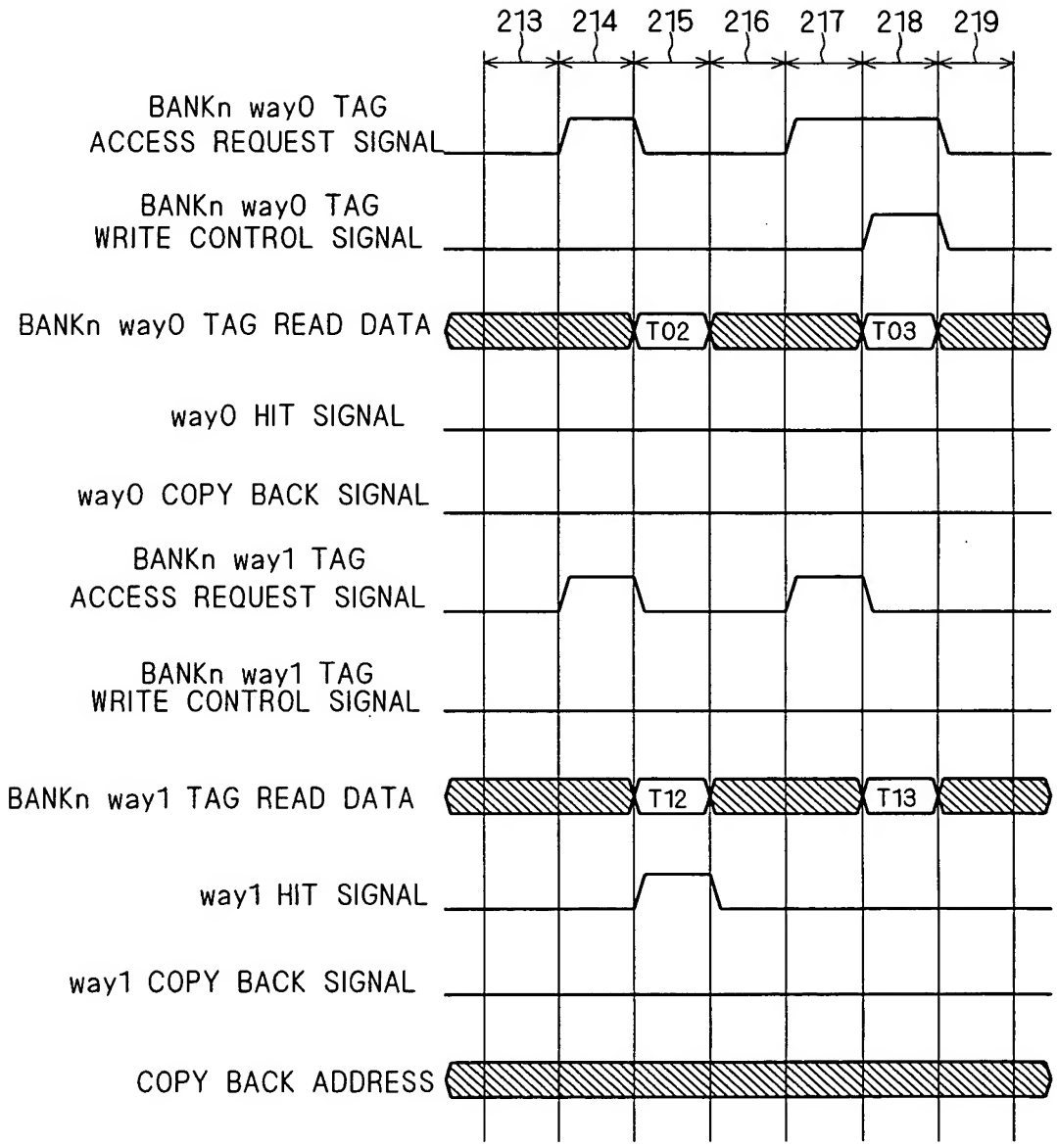

213
214
215
216
217
218
219
A2
A3
11011
11100
11000
11001
CLOCK SIGNAL
CACHE ADDRESS
BANKn STATUS ACCESS REQUEST SIGNAL
BANKn STATUS WRITE CONTROL SIGNAL
STATUS WRITE DATA
BANKn STATUS READ DATA

FIG. 14


213
214
215
216
217
218
219
BANKn way0 TAG ACCESS REQUEST SIGNAL
BANKn way0 TAG WRITE CONTROL SIGNAL
BANKn way0 TAG READ DATA
T02
T03
way0 HIT SIGNAL
way0 COPY BACK SIGNAL
BANKn way1 TAG ACCESS REQUEST SIGNAL
BANKn way1 TAG WRITE CONTROL SIGNAL
BANKn way1 TAG READ DATA
T12
T13
way1 HIT SIGNAL
way1 COPY BACK SIGNAL
COPY BACK ADDRESS

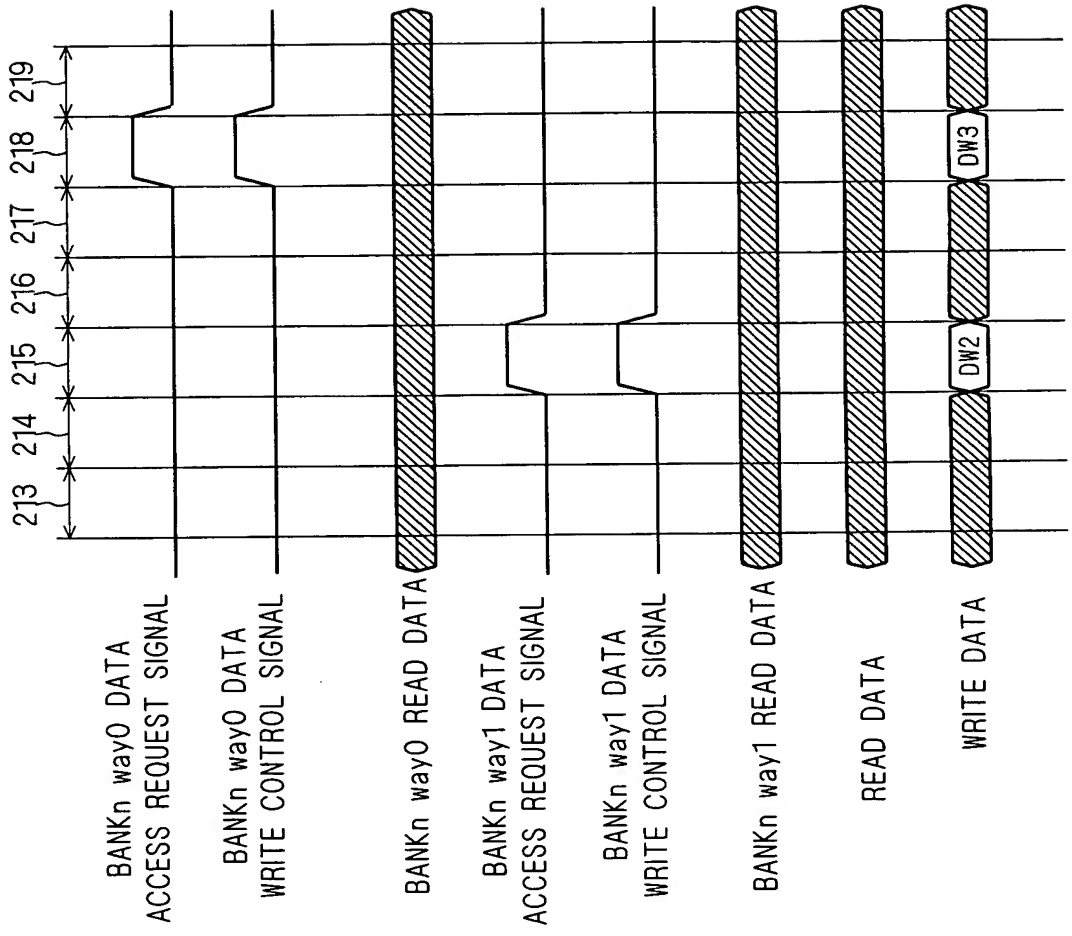

213
214
215
216
217
218
219
BANKn way0 DATA ACCESS REQUEST SIGNAL
BANKn way0 DATA WRITE CONTROL SIGNAL
BANKn way0 READ DATA
BANKn way1 DATA ACCESS REQUEST SIGNAL
BANKn way1 DATA WRITE CONTROL SIGNAL
BANKn way1 READ DATA
READ DATA
WRITE DATA
DW2
DW3

FIG. 15

FIG. 16

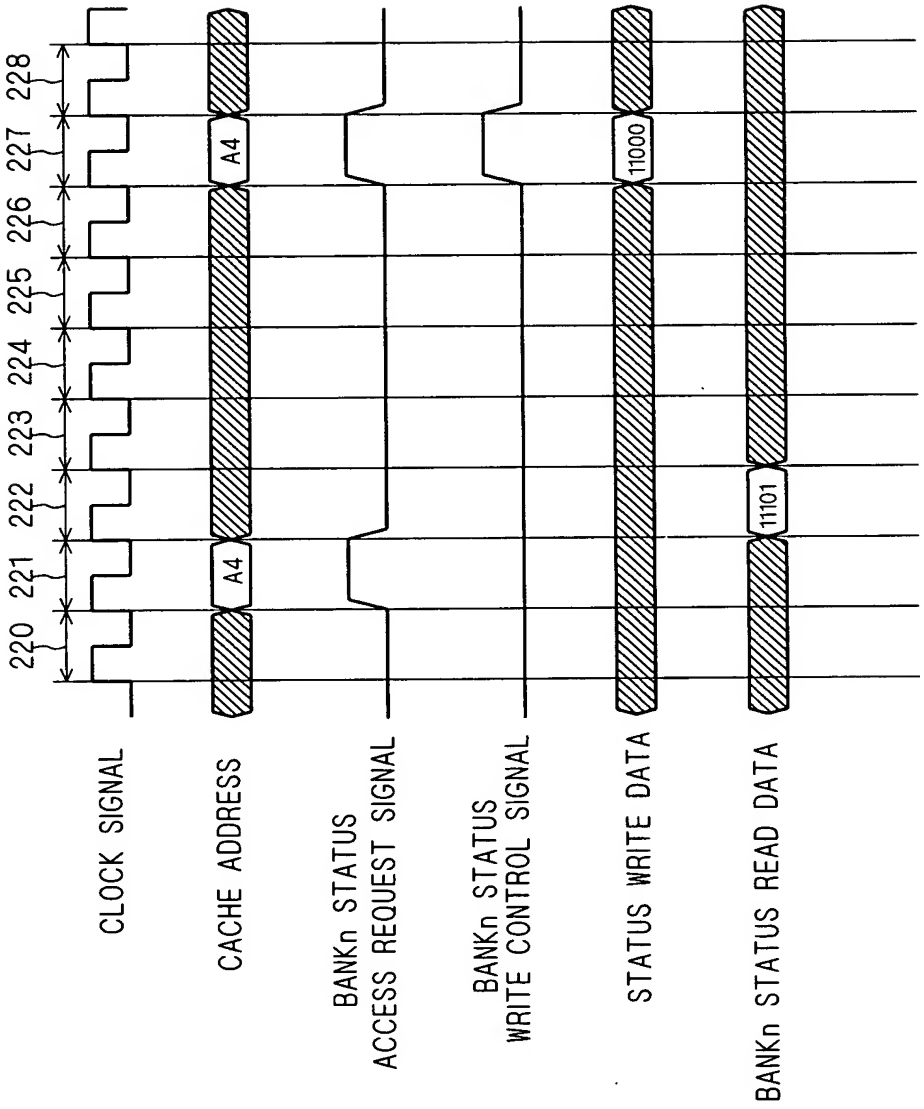

220
221
222
223
224
225
226
227
228
A4
A4
11000
11101
CLOCK SIGNAL
CACHE ADDRESS
BANKn STATUS
ACCESS REQUEST SIGNAL
BANKn STATUS
WRITE CONTROL SIGNAL
STATUS WRITE DATA
BANKn STATUS READ DATA

FIG. 17

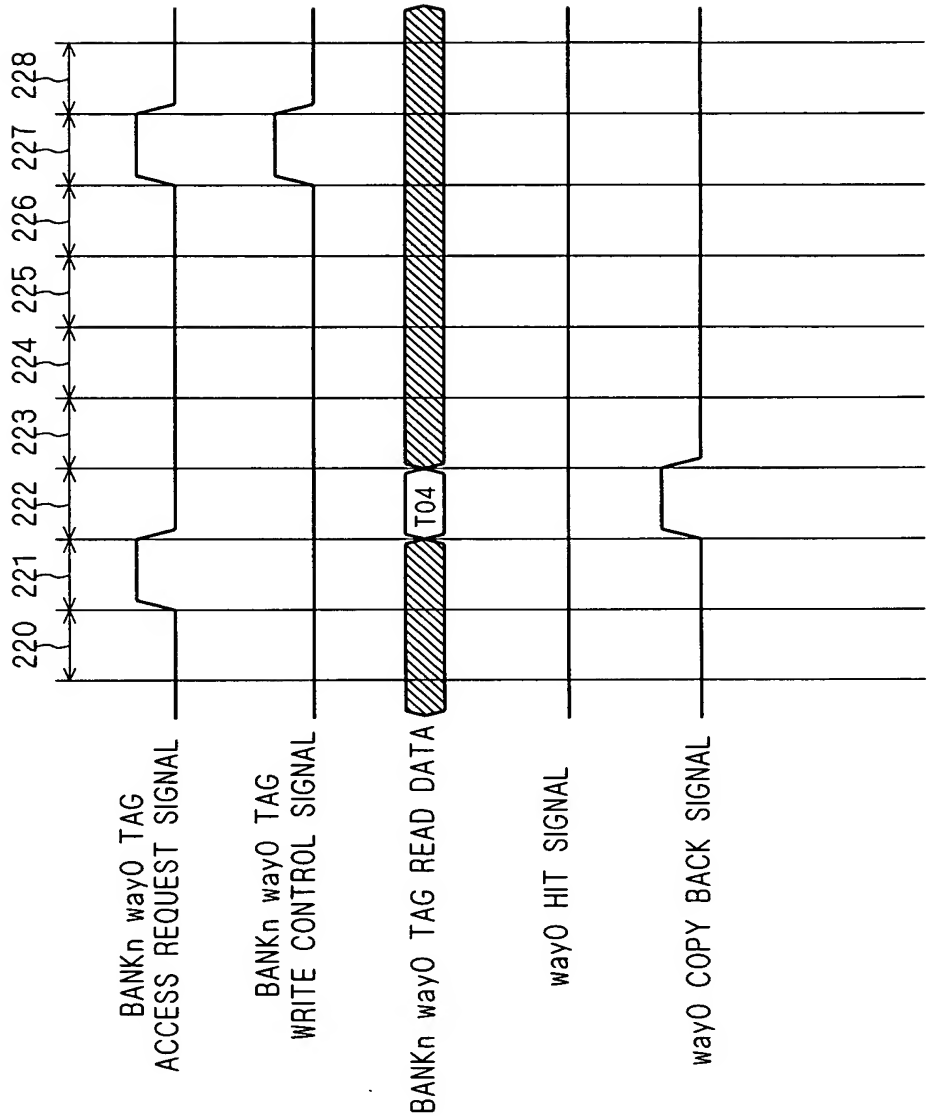
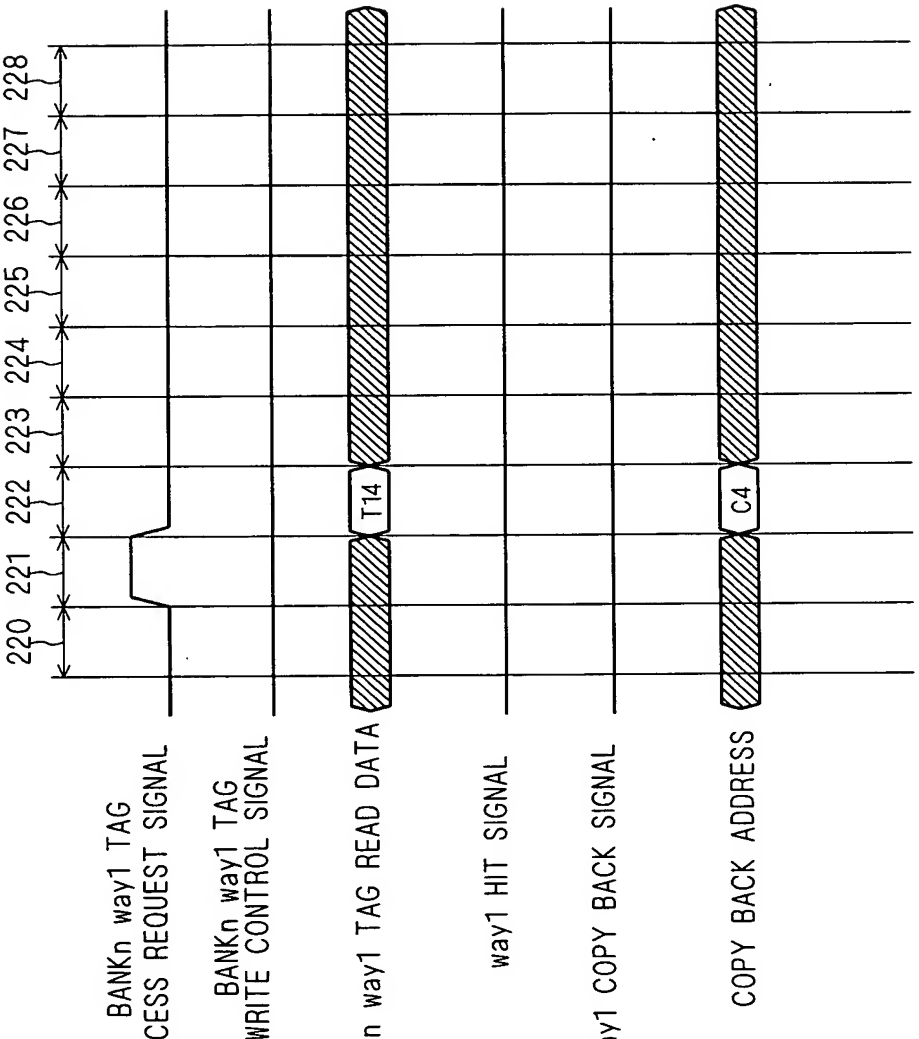

220
221
222
223
224
225
226
227
228
T04
BANKn way0 TAG
ACCESS REQUEST SIGNAL
BANKn way0 TAG
WRITE CONTROL SIGNAL
BANKn way0 TAG READ DATA
way0 HIT SIGNAL
way0 COPY BACK SIGNAL

FIG. 18


220
221
222
223
224
225
226
227
228
BANKn way1 TAG ACCESS REQUEST SIGNAL
BANKn way1 TAG WRITE CONTROL SIGNAL
BANKn way1 TAG READ DATA
T14
way1 HIT SIGNAL
way1 COPY BACK SIGNAL
COPY BACK ADDRESS
C4

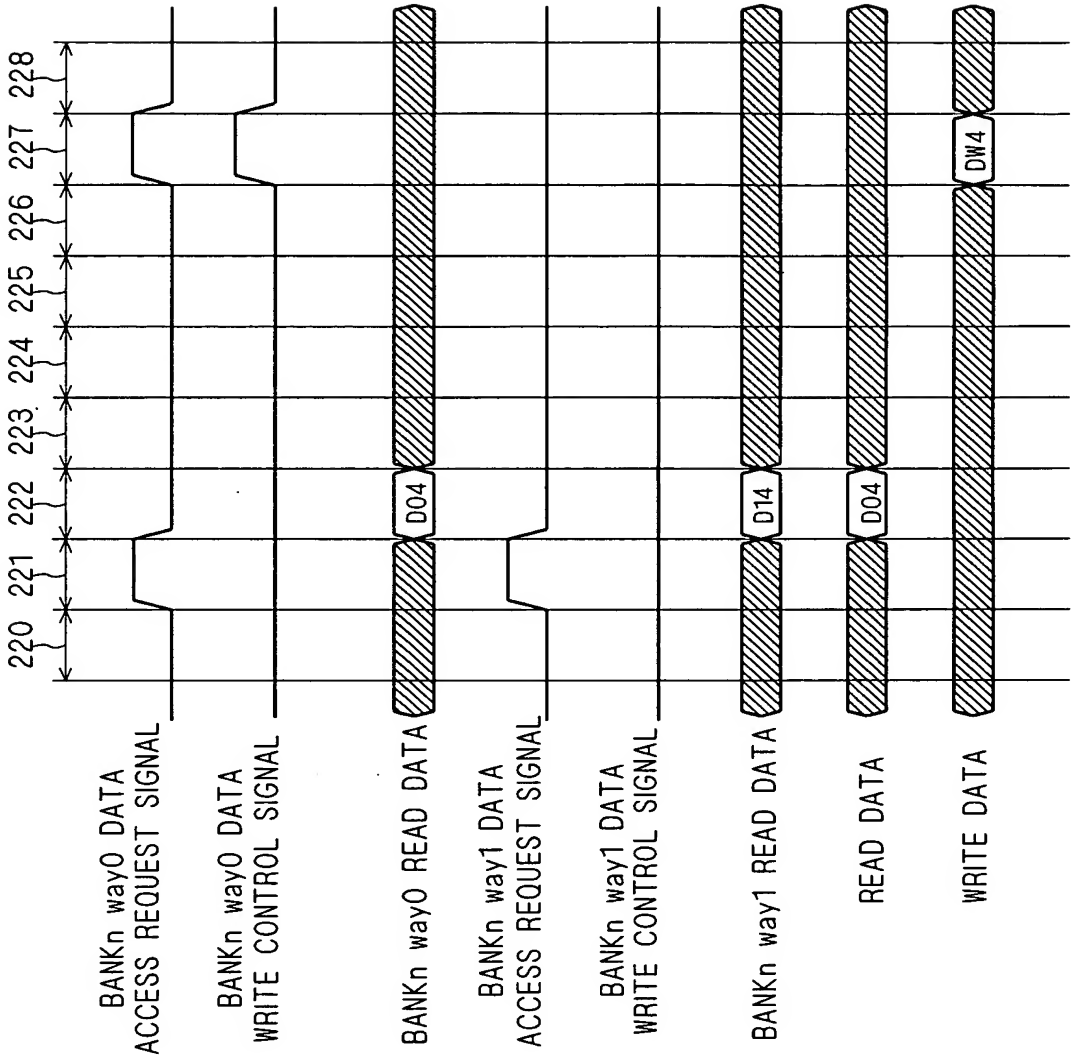
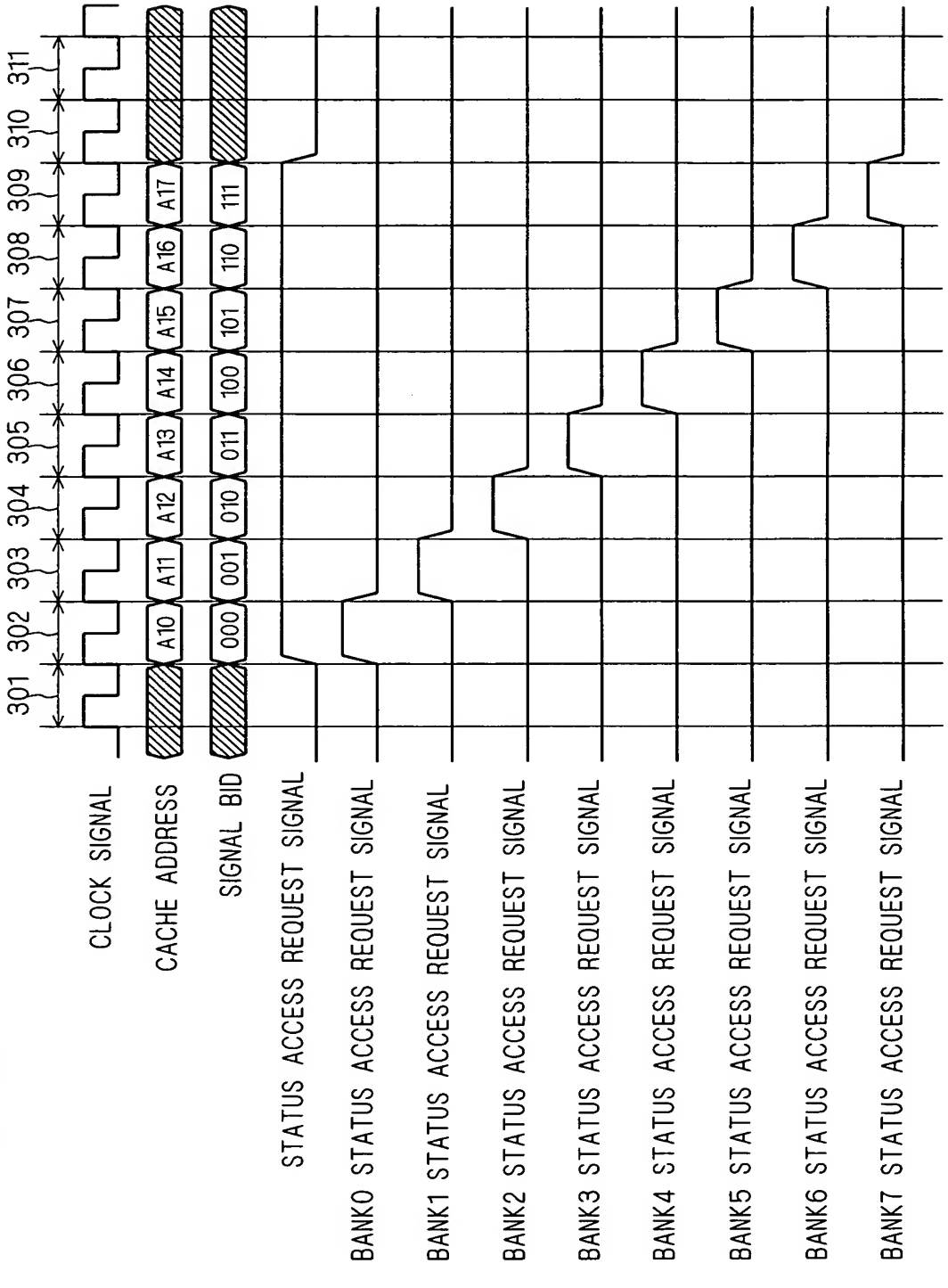

220
221
222
223
224
225
226
227
228
BANKn way0 DATA ACCESS REQUEST SIGNAL
BANKn way0 DATA WRITE CONTROL SIGNAL
BANKn way0 READ DATA
BANKn way1 DATA ACCESS REQUEST SIGNAL
BANKn way1 DATA WRITE CONTROL SIGNAL
BANKn way1 READ DATA
READ DATA
WRITE DATA
D04
D14
D04
DW4

FIG. 19

FIG. 20


301
302
303
304
305
306
307
308
309
310
311
CLOCK SIGNAL
CACHE ADDRESS
A10
A11
A12
A13
A14
A15
A16
A17
SIGNAL BID
000
001
010
011
100
101
110
111
STATUS ACCESS REQUEST SIGNAL
BANK0 STATUS ACCESS REQUEST SIGNAL
BANK1 STATUS ACCESS REQUEST SIGNAL
BANK2 STATUS ACCESS REQUEST SIGNAL
BANK3 STATUS ACCESS REQUEST SIGNAL
BANK4 STATUS ACCESS REQUEST SIGNAL
BANK5 STATUS ACCESS REQUEST SIGNAL
BANK6 STATUS ACCESS REQUEST SIGNAL
BANK7 STATUS ACCESS REQUEST SIGNAL

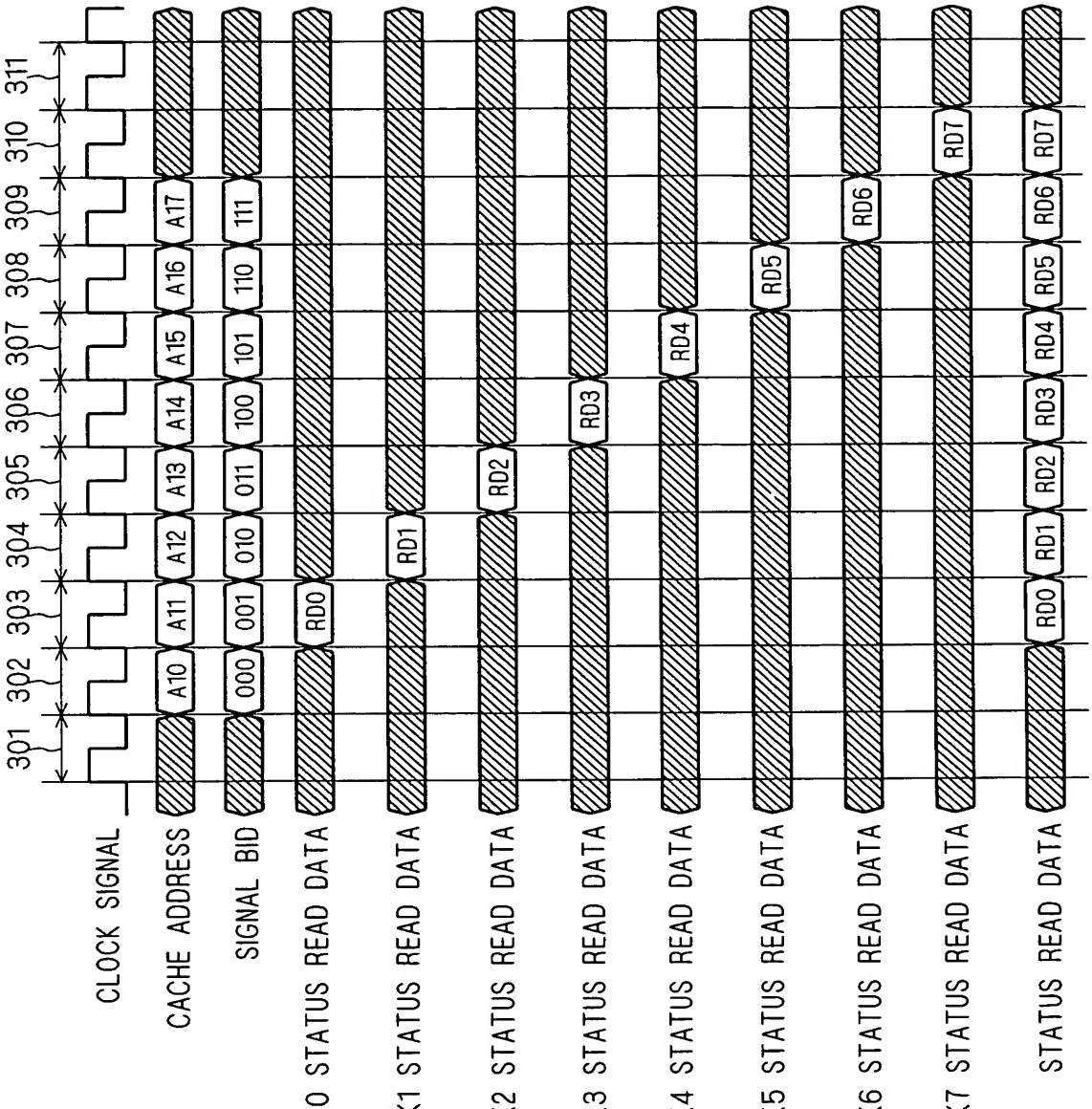

301
302
303
304
305
306
307
308
309
310
311
CLOCK SIGNAL
CACHE ADDRESS
SIGNAL BID
BANK0 STATUS READ DATA
BANK1 STATUS READ DATA
BANK2 STATUS READ DATA
BANK3 STATUS READ DATA
BANK4 STATUS READ DATA
BANK5 STATUS READ DATA
BANK6 STATUS READ DATA
BANK7 STATUS READ DATA
STATUS READ DATA
A10
A11
A12
A13
A14
A15
A16
A17
000
001
010
011
100
101
110
111
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7

FIG. 21

FIG. 22

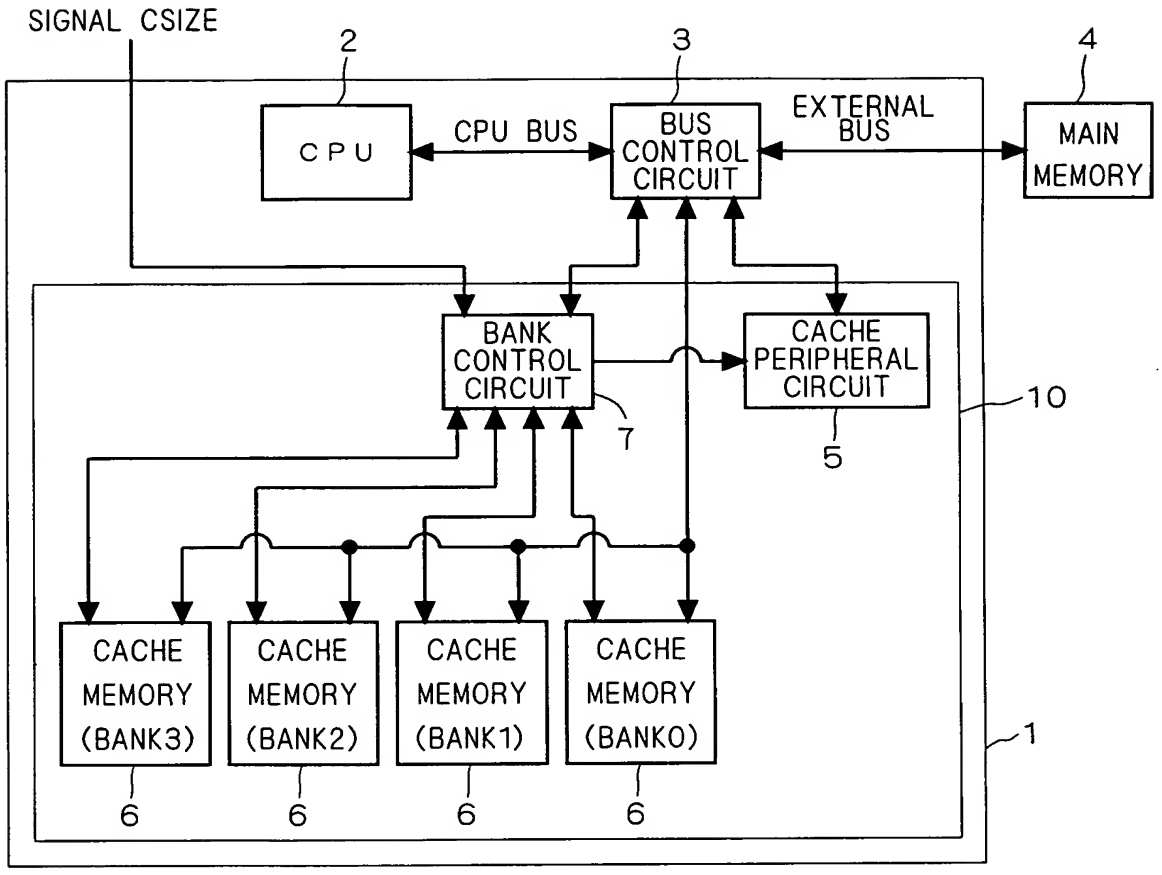

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANK3)
CACHE MEMORY (BANK2)
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK0)
6
6
6
6
1

FIG. 23

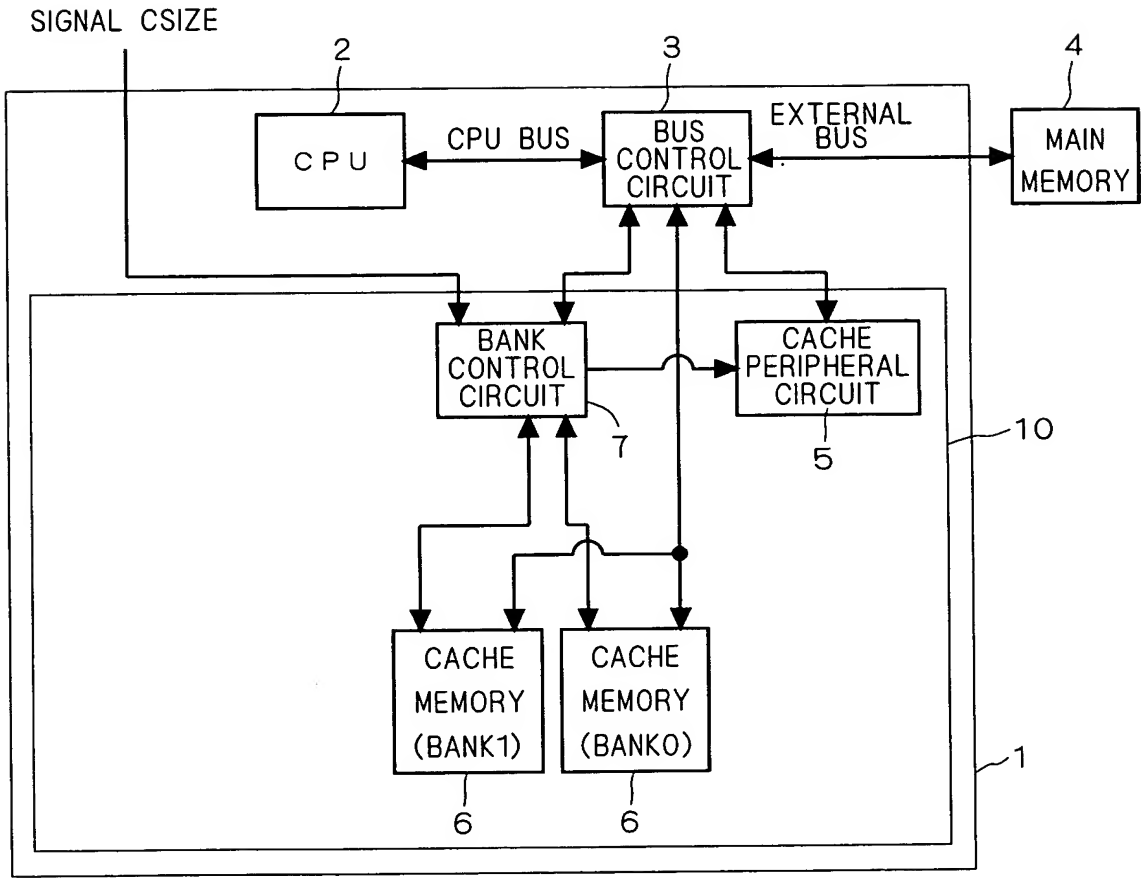

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANK1)
6
CACHE MEMORY (BANK0)
6
1

FIG. 24

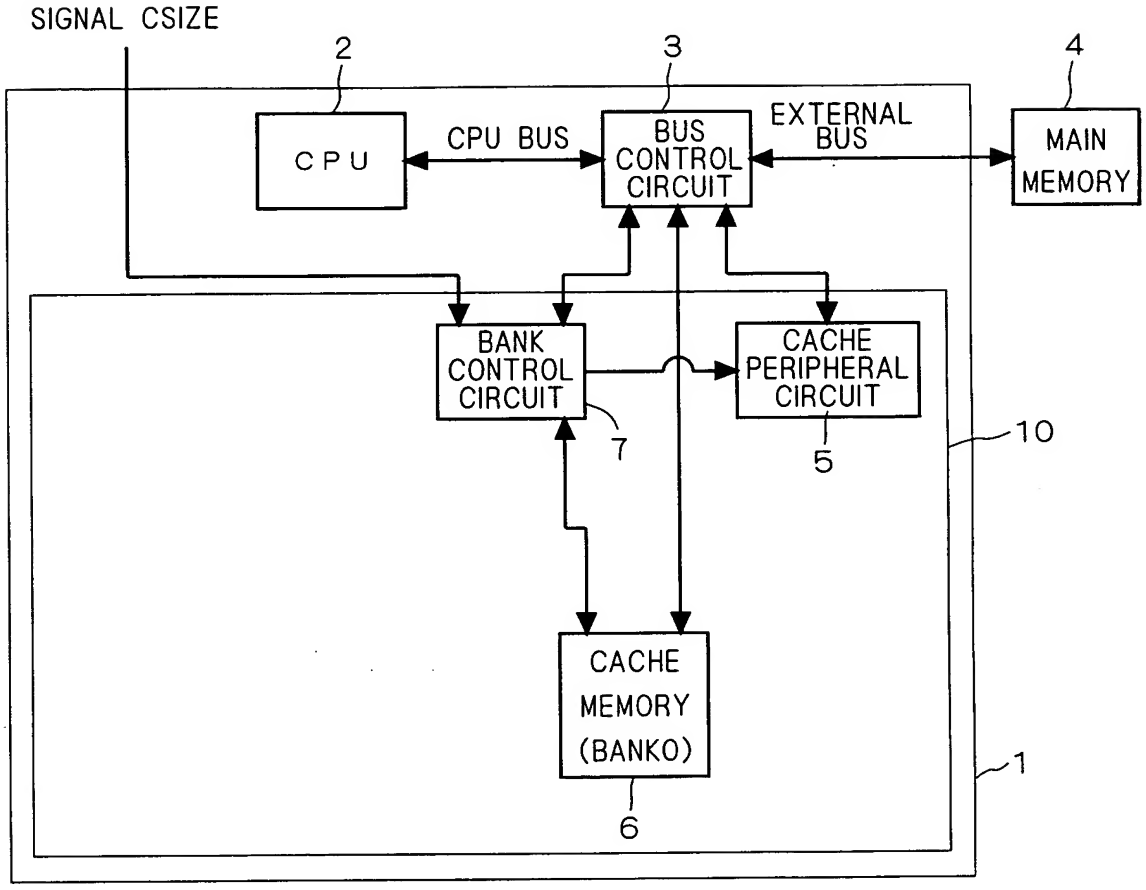

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANKO)
6
1

FIG. 25

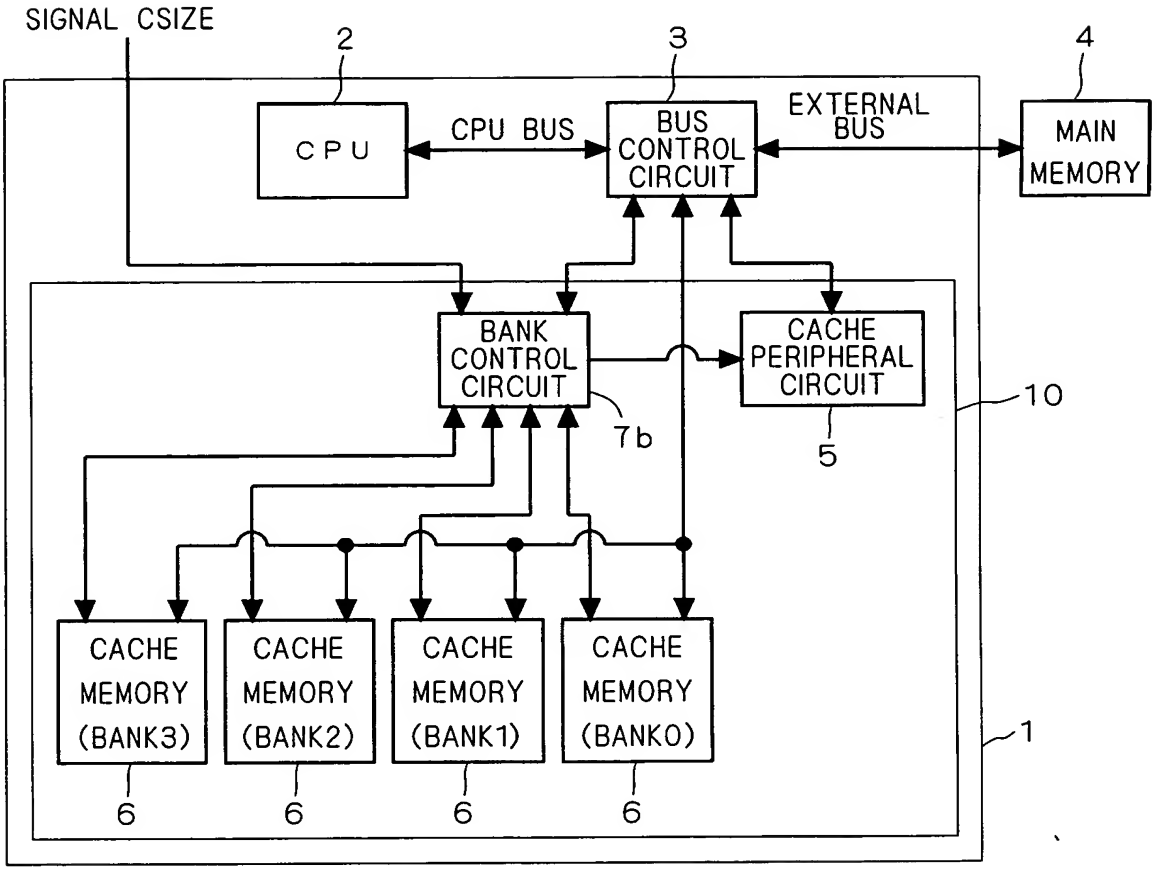

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7b
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANK3)
CACHE MEMORY (BANK2)
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK0)
6
6
6
6
1

FIG. 26

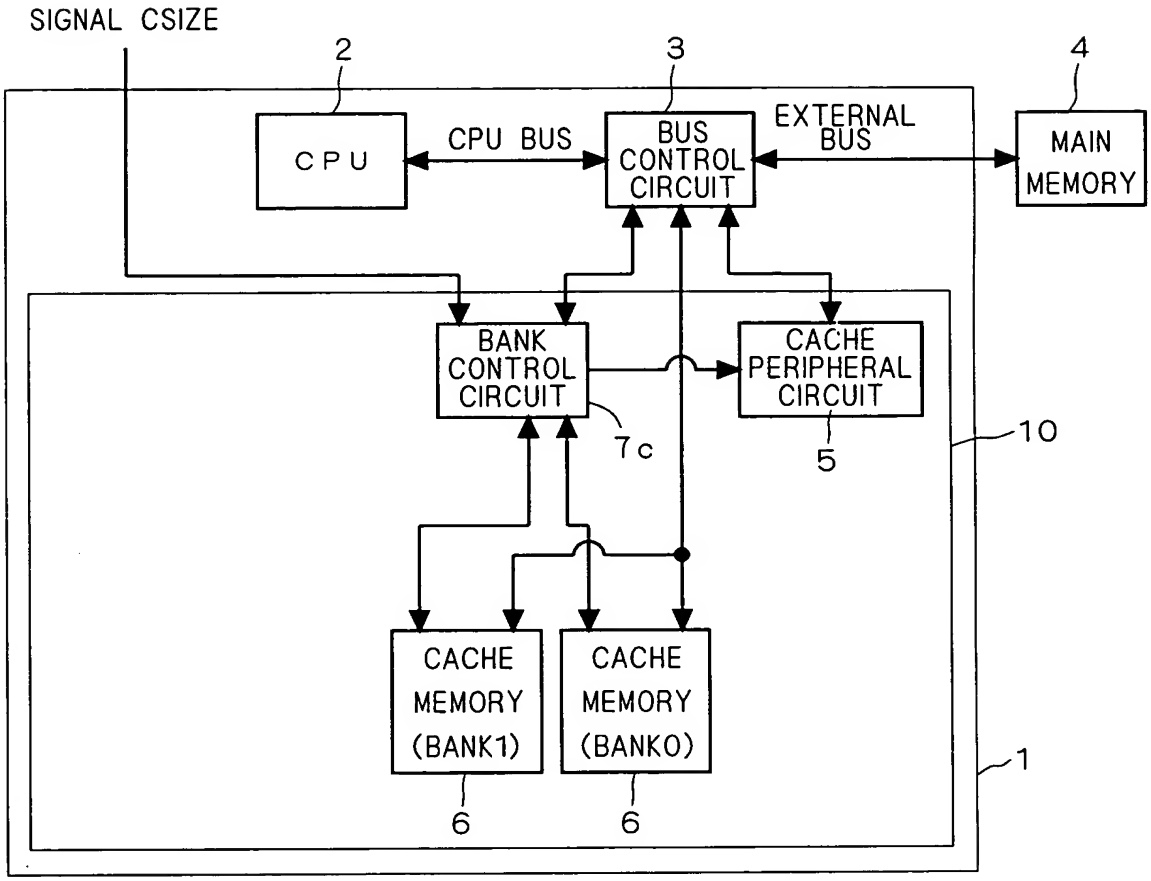

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7c
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK0)
6
6
1

FIG. 27

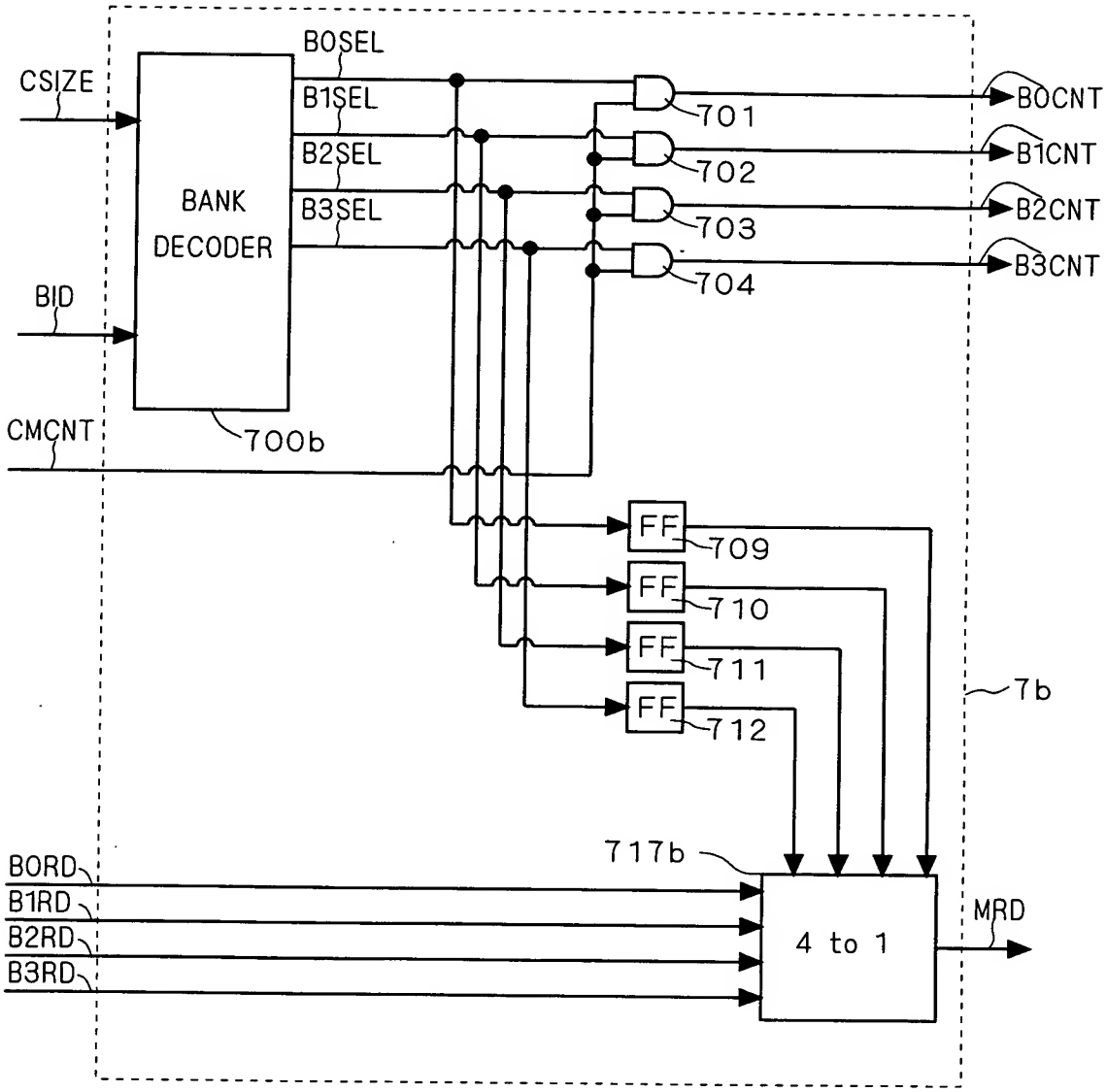

CSIZE
BID
CMCNT
BANK DECODER
700b
B0SEL
B1SEL
B2SEL
B3SEL
701
702
703
704
B0CNT
B1CNT
B2CNT
B3CNT
FF
709
FF
710
FF
711
FF
712
7b
717b
B0RD
B1RD
B2RD
B3RD
4 to 1
MRD

FIG. 28

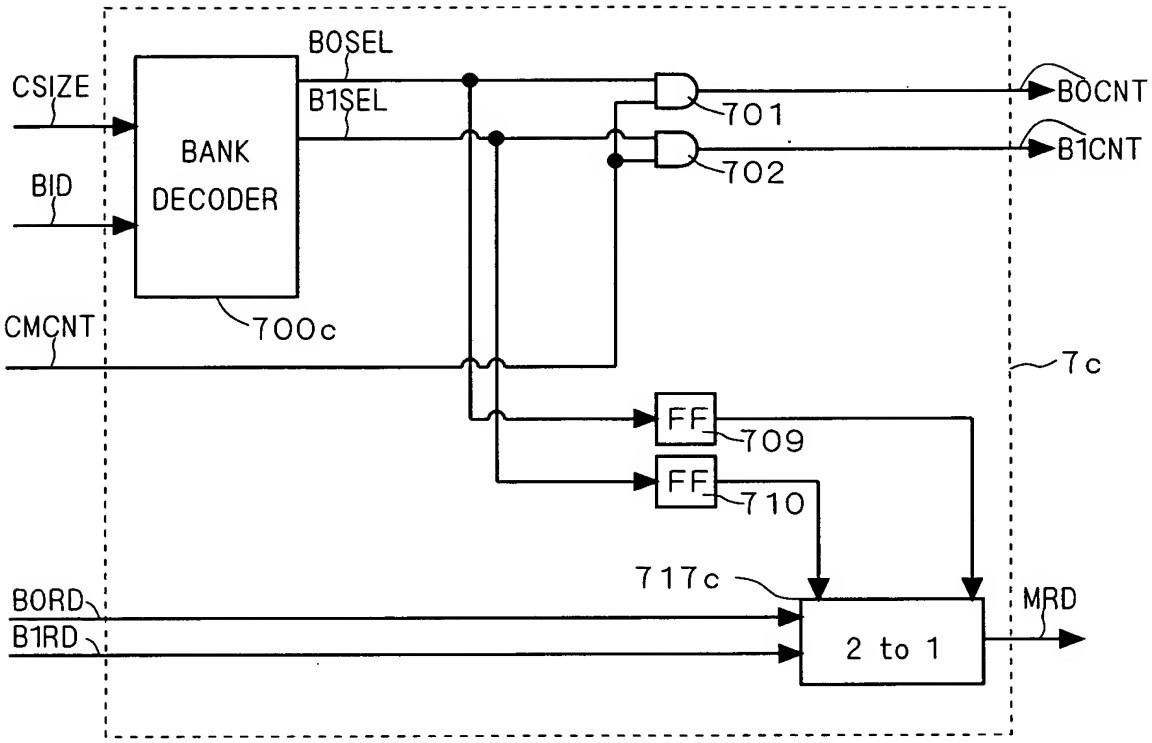

CSIZE
BID
CMCNT
BANK DECODER
700c
B0SEL
B1SEL
701
702
B0CNT
B1CNT
7c
FF
709
FF
710
717c
B0RD
B1RD
2 to 1
MRD

FIG. 29

CSIZE	BID	BANK0 SELECTION SIGNAL	BANK1 SELECTION SIGNAL	BANK2 SELECTION SIGNAL	BANK3 SELECTION SIGNAL
00	000	1	0	0	0
	001	1	0	0	0
	010	1	0	0	0
	011	1	0	0	0
	100	1	0	0	0
	101	1	0	0	0
	110	1	0	0	0
	111	1	0	0	0
01	000	1	0	0	0
	001	0	1	0	0
	010	1	0	0	0
	011	0	1	0	0
	100	1	0	0	0
	101	0	1	0	0
	110	1	0	0	0
	111	0	1	0	0
10	000	1	0	0	0
	001	0	1	0	0
	010	0	0	1	0
	011	0	0	0	1
	100	1	0	0	0
	101	0	1	0	0
	110	0	0	1	0
	111	0	0	0	1

FIG. 30

CSIZE	BID	BANK0 SELECTION SIGNAL	BANK1 SELECTION SIGNAL
00	000	1	0
	001	1	0
	010	1	0
	011	1	0
	100	1	0
	101	1	0
	110	1	0
	111	1	0
01	000	1	0
	001	0	1
	010	1	0
	011	0	1
	100	1	0
	101	0	1
	110	1	0
	111	0	1

FIG. 31

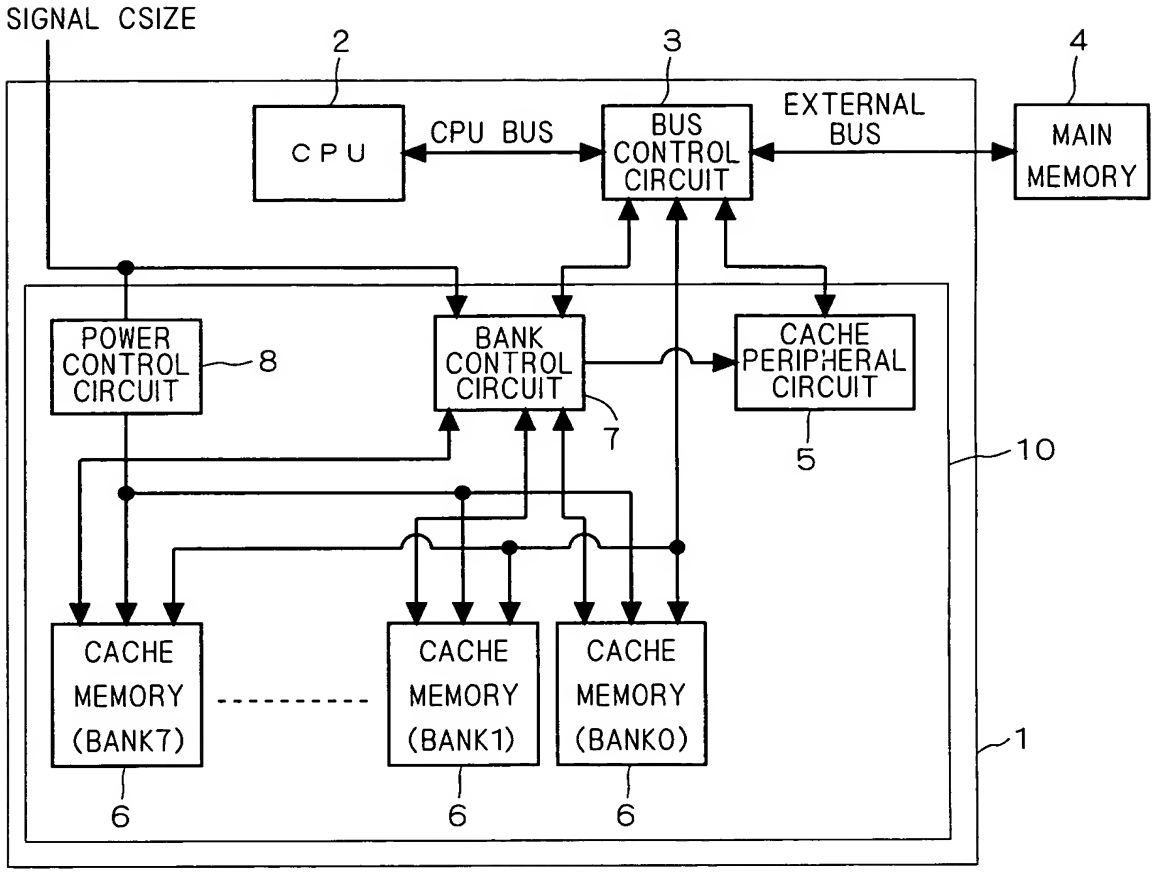

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
POWER CONTROL CIRCUIT
8
BANK CONTROL CIRCUIT
7
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANK7)
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK0)
6
6
6
1

FIG. 32

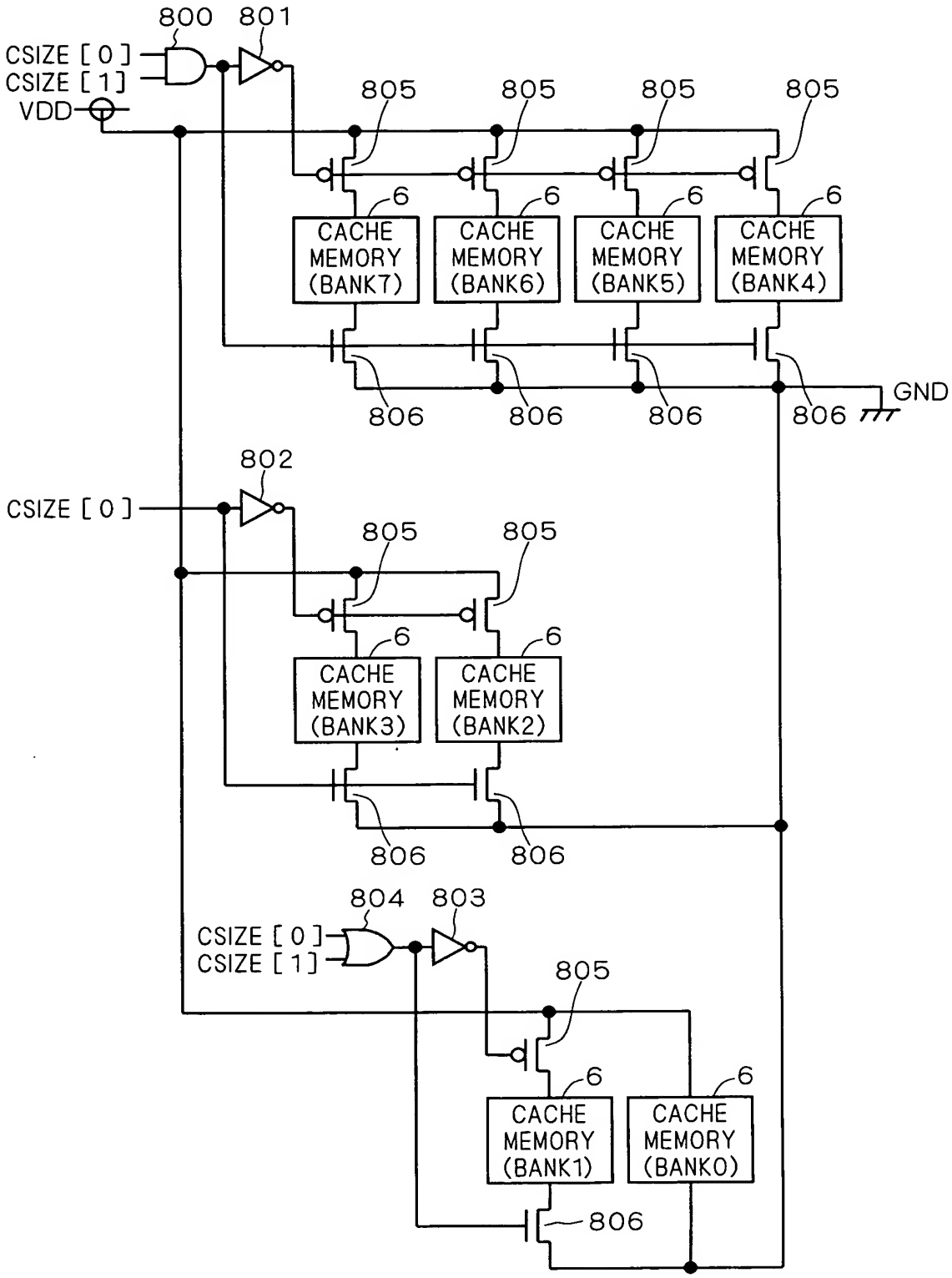

800
801
CSIZE [0]
CSIZE [1]
VDD
805
805
805
805
6
6
6
6
CACHE MEMORY (BANK7)
CACHE MEMORY (BANK6)
CACHE MEMORY (BANK5)
CACHE MEMORY (BANK4)
806
806
806
806
GND
802
CSIZE [0]
805
805
6
6
CACHE MEMORY (BANK3)
CACHE MEMORY (BANK2)
806
806
804
803
CSIZE [0]
CSIZE [1]
805
6
6
CACHE MEMORY (BANK1)
CACHE MEMORY (BANK0)
806

FIG. 33

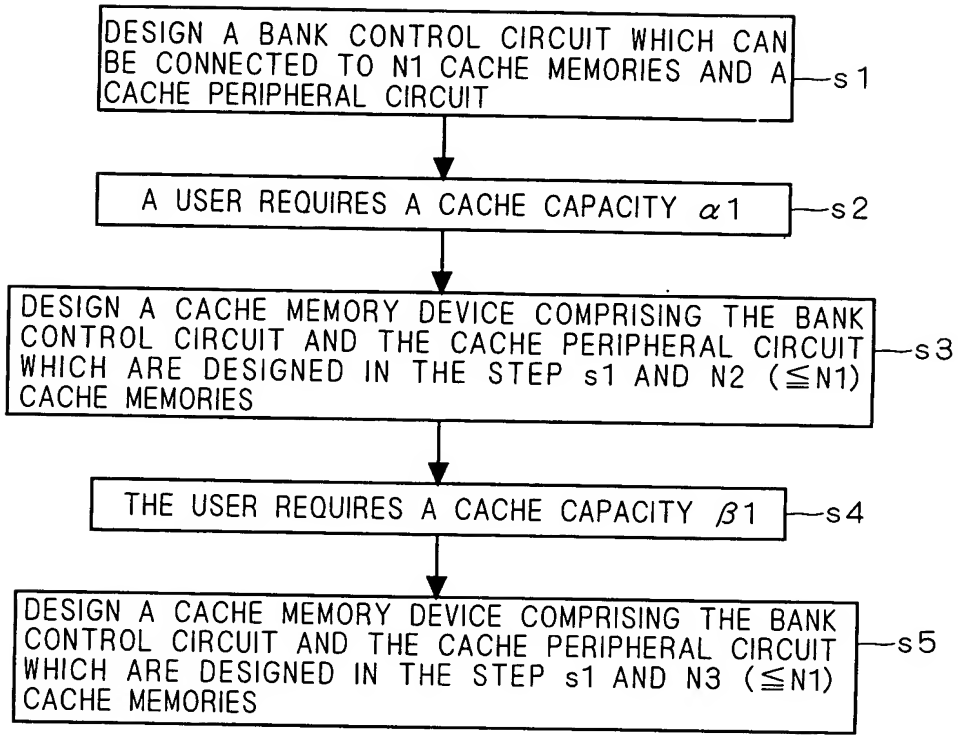

DESIGN A BANK CONTROL CIRCUIT WHICH CAN BE CONNECTED TO N1 CACHE MEMORIES AND A CACHE PERIPHERAL CIRCUIT
s1
A USER REQUIRES A CACHE CAPACITY α1
s2
DESIGN A CACHE MEMORY DEVICE COMPRISING THE BANK CONTROL CIRCUIT AND THE CACHE PERIPHERAL CIRCUIT WHICH ARE DESIGNED IN THE STEP s1 AND N2 (≦N1) CACHE MEMORIES
s3
THE USER REQUIRES A CACHE CAPACITY β1
s4
DESIGN A CACHE MEMORY DEVICE COMPRISING THE BANK CONTROL CIRCUIT AND THE CACHE PERIPHERAL CIRCUIT WHICH ARE DESIGNED IN THE STEP s1 AND N3 (≦N1) CACHE MEMORIES
s5

FIG. 34

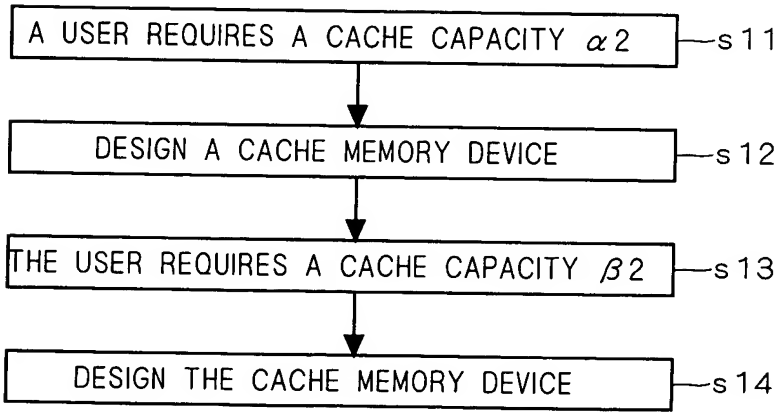

A USER REQUIRES A CACHE CAPACITY α2
s11
DESIGN A CACHE MEMORY DEVICE
s12
THE USER REQUIRES A CACHE CAPACITY β2
s13
DESIGN THE CACHE MEMORY DEVICE
s14

FIG. 35

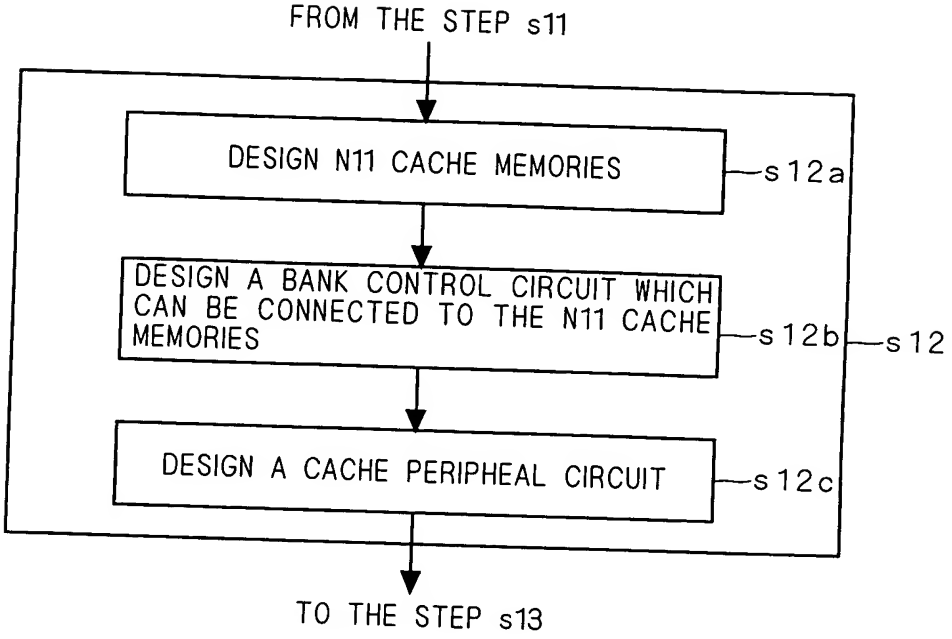

FROM THE STEP s11
DESIGN N11 CACHE MEMORIES
s12a
DESIGN A BANK CONTROL CIRCUIT WHICH CAN BE CONNECTED TO THE N11 CACHE MEMORIES
s12b
s12
DESIGN A CACHE PERIPHEAL CIRCUIT
s12c
TO THE STEP s13

FIG. 36

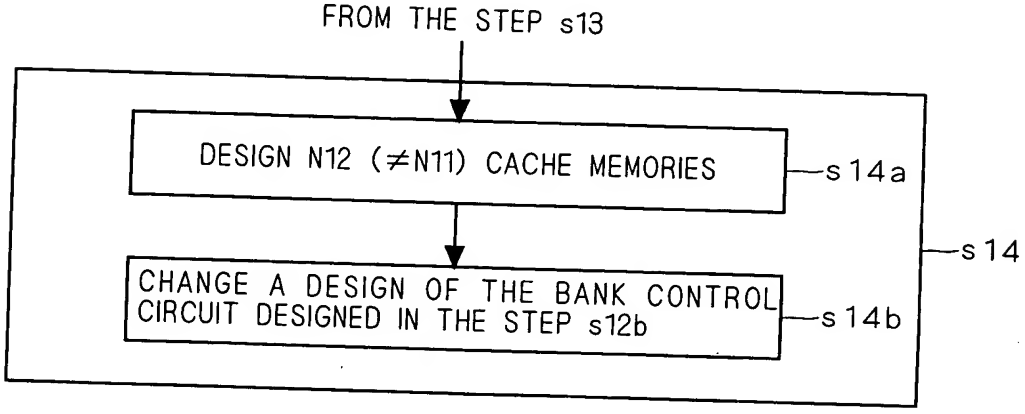

FROM THE STEP s13
DESIGN N12 (≠N11) CACHE MEMORIES
s14a
s14
CHANGE A DESIGN OF THE BANK CONTROL CIRCUIT DESIGNED IN THE STEP s12b
s14b

FIG. 37

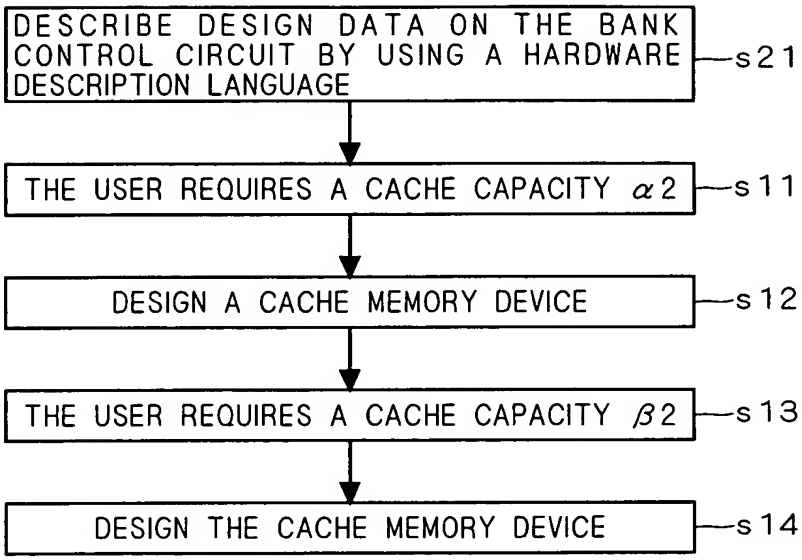

DESCRIBE DESIGN DATA ON THE BANK CONTROL CIRCUIT BY USING A HARDWARE DESCRIPTION LANGUAGE
s21
THE USER REQUIRES A CACHE CAPACITY α2
s11
DESIGN A CACHE MEMORY DEVICE
s12
THE USER REQUIRES A CACHE CAPACITY β2
s13
DESIGN THE CACHE MEMORY DEVICE
s14

FIG. 38

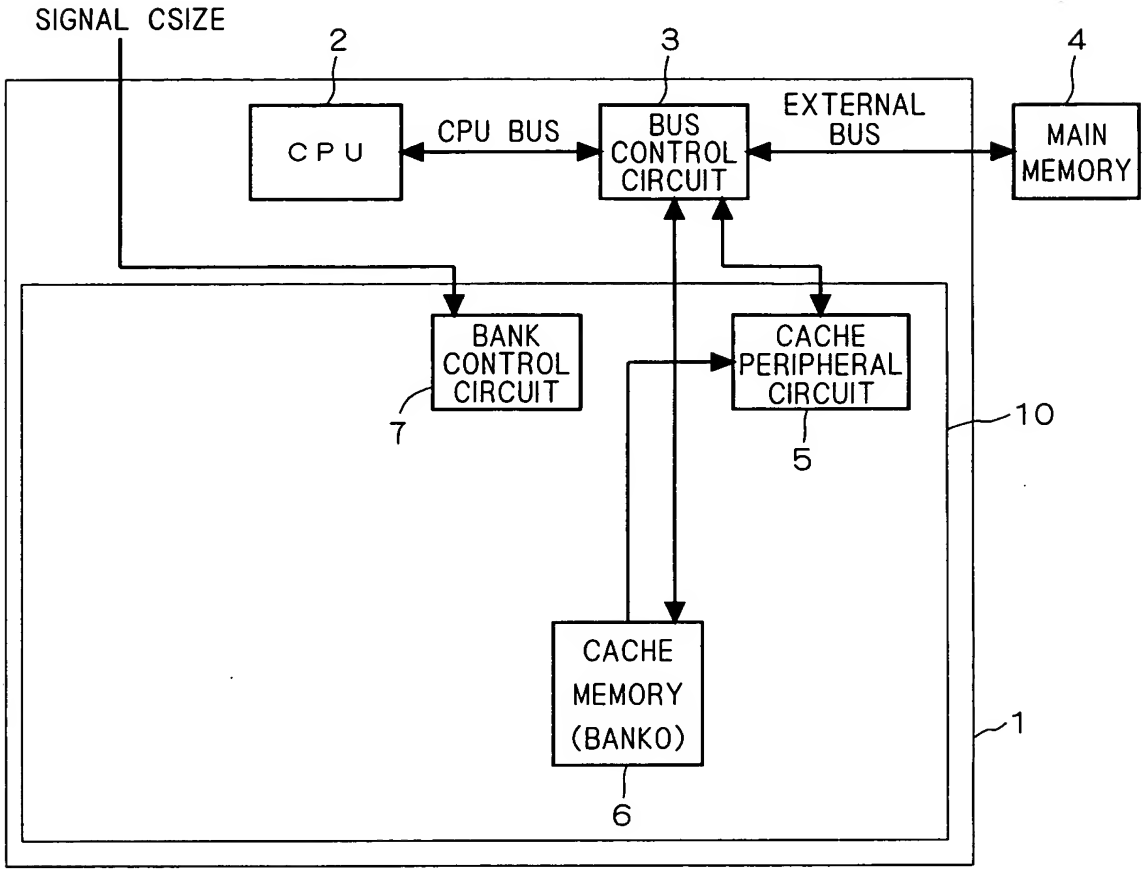
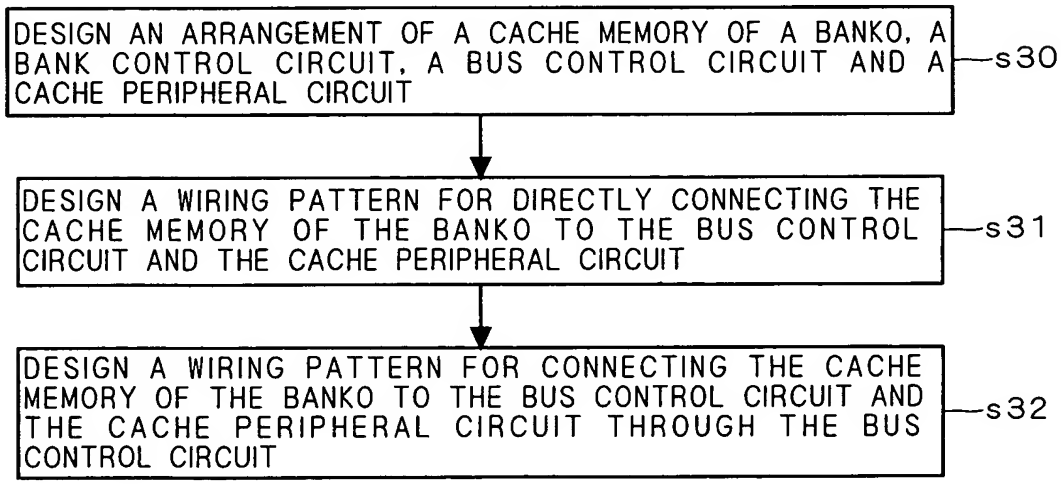

SIGNAL CSIZE
2
3
4
CPU
CPU BUS
BUS CONTROL CIRCUIT
EXTERNAL BUS
MAIN MEMORY
BANK CONTROL CIRCUIT
7
CACHE PERIPHERAL CIRCUIT
5
10
CACHE MEMORY (BANKO)
6
1

FIG. 39


DESIGN AN ARRANGEMENT OF A CACHE MEMORY OF A BANKO, A BANK CONTROL CIRCUIT, A BUS CONTROL CIRCUIT AND A CACHE PERIPHERAL CIRCUIT
s30
DESIGN A WIRING PATTERN FOR DIRECTLY CONNECTING THE CACHE MEMORY OF THE BANKO TO THE BUS CONTROL CIRCUIT AND THE CACHE PERIPHERAL CIRCUIT
s31
DESIGN A WIRING PATTERN FOR CONNECTING THE CACHE MEMORY OF THE BANKO TO THE BUS CONTROL CIRCUIT AND THE CACHE PERIPHERAL CIRCUIT THROUGH THE BUS CONTROL CIRCUIT
s32